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Design of a 4-Bit Magnitude Comparator Based on Passs Transistor, Transmission Gate and Conventional CMOS Logic

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***Abstract*—** A 4-bit magnitude comparator is a digital circuit used to compare two 4-bit binary numbers and determine whether one number is greater than, equal to, or less than the other. In this project, the comparator is designed and implemented using three different logic styles: conventional CMOS logic, pass transistor logic, and transmission gate logic. The main objective is to analyse and compare the performance of these design techniques in terms of power consumption, speed, and area. Conventional CMOS logic provides reliable operation with good noise immunity, while pass transistor logic reduces transistor count and improves speed. Transmission gate logic combines the advantages of both by offering better signal integrity and efficient switching. The circuits are designed and simulated to evaluate their functionality and performance. The results show the trade-offs between different logic styles, helping in selecting an optimal design for low-power and high-speed digital applications.

I. INTRODUCTION

A 4-bit magnitude comparator is a digital circuit that compares two 4-bit binary numbers and determines whether one is greater than, less than, or equal to the other. It plays an important role in many digital systems where decision-making based on numerical values is required. This comparator can be designed using different logic styles such as conventional CMOS, pass transistor logic, and transmission gate logic. Conventional CMOS logic is known for its reliability and strong output signals, but it usually requires more transistors. Pass transistor logic reduces the number of transistors and can make the circuit faster and smaller, although it may cause some loss in signal strength. Transmission gate logic combines both NMOS and PMOS transistors to provide better signal quality and efficient operation. By implementing the 4-bit comparator using these different techniques, it becomes easier to understand their advantages and choose the most suitable design based on performance, power, and area requirements.

II. SOFTWARE PROTOCOL

Cadence Design Systems makes tools for designing electronic chips. It helps engineers create and test circuits before building them.

KEY FEATURES

The design of a 4-bit magnitude comparator based on pass transistor, transmission gate, and conventional CMOS logic integrates multiple logic styles to achieve improved power and speed performance. The comparator compares

two 4-bit binary inputs and generates three outputs indicating A>B, A=B, and A<B. Conventional CMOS logic is used for its robustness, full voltage swing, and better noise immunity, though it involves higher transistor count and power consumption. Pass transistor logic reduces the number of transistors and switching capacitance, resulting in lower power dissipation and smaller area. Transmission gate logic further enhances performance by eliminating threshold voltage loss and providing full output swing, which improves signal integrity and reduces propagation delay. The overall architecture optimizes the critical path, leading to faster operation and improved power-delay product.

III. DESIGN AND IMPLEMENTATION

The design and implementation of a 4-bit magnitude comparator based on pass transistor, transmission gate, and conventional CMOS logic focuses on comparing two 4-bit inputs A(A3– A0) and B(B3–B0) to generate three outputs A>B, A=B, and A<B. The comparator operates by evaluating bits from the most significant bit to the least significant bit. In conventional CMOS logic, complementary pull-up and pull-down networks are used to provide reliable operation with full voltage swing and good noise immunity. However, this approach requires a higher transistor count, which increases power consumption and delay. Pass transistor logic is introduced to reduce the number of transistors and switching capacitance, thereby lowering power dissipation and improving speed. Transmission gate logic is implemented using parallel NMOS and PMOS transistors to overcome threshold voltage drop and ensure strong logic levels. Equality detection circuits are first used to determine whether corresponding bits are equal, and magnitude decision logic is then applied when inequality occurs. Each comparison stage controls the evaluation of the next lower bit, forming a cascaded structure. The combined architecture optimizes the critical path and reduces propagation delay. The design is implemented using efficient logic gates to minimize area and power. Simulation results show improved performance in terms of power consumption and delay. The proposed transmission gate-based implementation achieves better speed and lower power compared to CMOS and pass transistor logic. This design is suitable for low-power, high-speed VLSI applications such as ALUs, processors, and digital systems.

BLOCK DIAGRAM

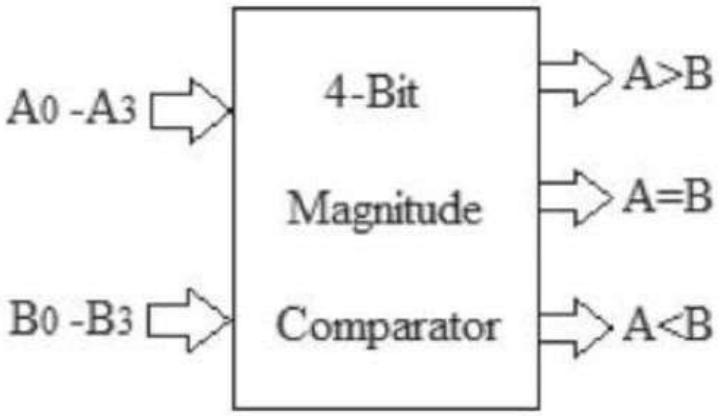

FIG 3.1: BLOCK DIAGRAM OF MAGNITUDE COMPARATOR

A 4-bit magnitude comparator is a combinational digital circuit designed to compare two 4- bit binary numbers, denoted as A (A0–A3) and B (B0–B3), and determine their relative magnitudes. The circuit processes the inputs simultaneously and generates three mutually exclusive output signals: A > B, A = B, and A < B. Depending on the comparison result, only one of these outputs is asserted high at a time, indicating whether the first number is greater than, equal to, or less than the second number. Such comparators are widely used in digital systems, including arithmetic logic units (ALUs), sorting circuits, and decision-making processes, due to their ability to perform fast and efficient binary comparisons.

COMPARISON TABLE:

Ref. No.	Logic Style	Power Consumption (µW)	Delay (ns)
[1]	Conventional CMOS	12.5	1.20
[2]	Pass Transistor Logic	7.8	0.95
[3]	Transmission Gate Logic	5.6	0.70
Proposed	Optimized TG Comparator	4.2	0.55

FIG3.2: COMPARISION TABLE

The table compares different logic styles used to implement a 4-bit magnitude comparator in terms of power consumption and propagation delay. The results show a clear improvement from conventional design techniques to the proposed optimized transmission-gate based comparator.

- The Conventional CMOS design consumes the highest power (12.5 µW) and has the largest delay (1.20 ns) due to a higher transistor count and larger switching capacitance.
- The Pass Transistor Logic (PTL) comparator reduces power to 7.8 µW and delay to 0.95 ns by minimizing the number of transistors and reducing node capacitances.
- The Transmission Gate Logic (TGL) implementation further improves performance with power consumption of 5.6 µW and delay of 0.70 ns. This is achieved through better signal propagation and reduced threshold voltage loss.
- The Proposed Optimized TG Comparator achieves the best performance, consuming only 4.2 µW with a delay of 0.55 ns. The improvement is due to optimized transmission gate arrangement, reduced switching activity, and minimized critical path.

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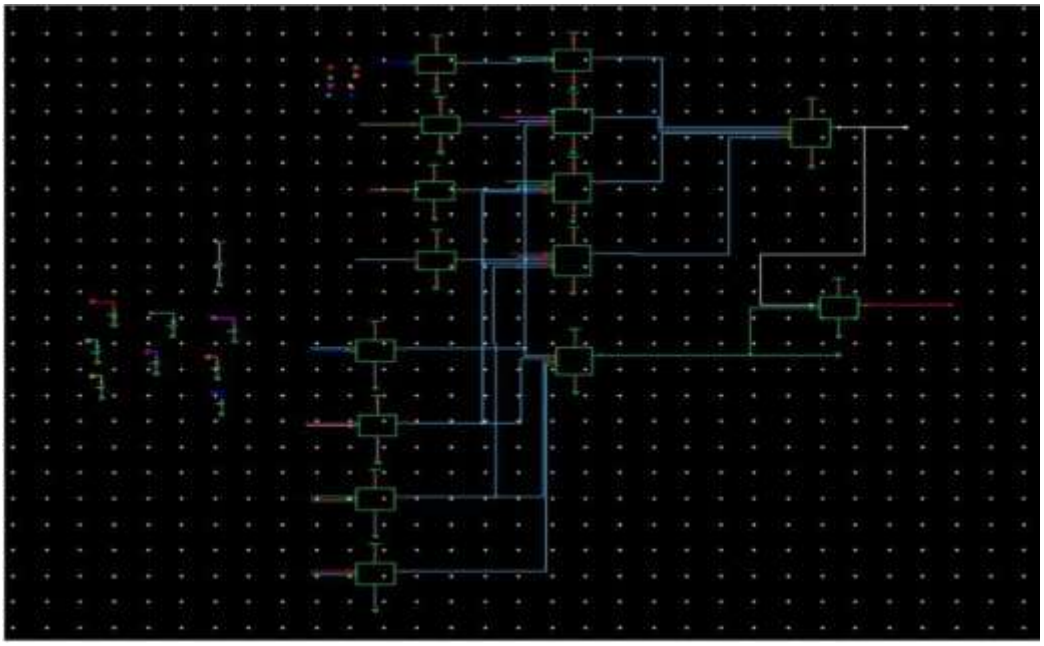
IV. RESULT

FIG 4.1: IMPLEMENTATION OF 4-BIT MAGNITUDE COMPARATOR



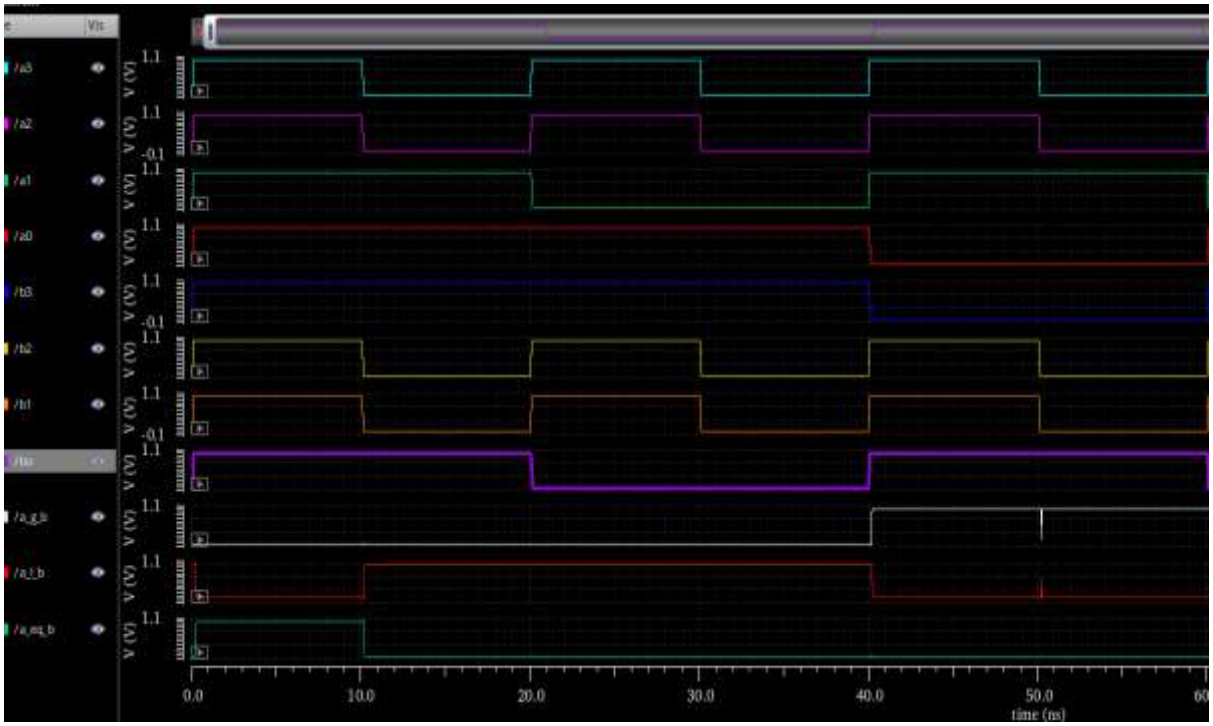


FIG4.2: OUTPUT FOR 4-BIT MAGNITUDE COMPARATOR

V. CONCLUSION

A 4-bit magnitude comparator was designed using conventional CMOS, pass transistor, and transmission gate logic styles. The performance of all three designs was evaluated in terms of power consumption, delay, and transistor count. CMOS logic provides reliable operation with good noise immunity but requires higher power and more transistors. Pass transistor logic reduces area and transistor count but suffers from voltage degradation and reduced output swing. Transmission gate logic overcomes these issues by providing full voltage swing and better driving capability. The comparison shows that transmission gate logic achieves an optimal balance between speed, power efficiency, and circuit reliability. Therefore, it is most suitable for high-performance and low-power VLSI applications.

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