



Performance Analysis of Carry Look-Ahead Adder using Hybrid Full Adder in 45nm Technology

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Abstract : This paper presents the design and performance analysis of a Carry Look-Ahead (CLA) adder using a Hybrid Full Adder (HFA) in 45 nm CMOS technology, aimed at achieving high speed and low power operation. The proposed design combines parallel carry generation of the CLA architecture with a reduced transistor hybrid full adder to minimize propagation delay and power consumption. The circuit is designed and simulated using Cadence Virtuoso, and key parameters such as delay, power, and power-delay product (PDP) are evaluated. Simulation results show that the proposed CLA adder achieves a propagation delay of 0.42 ns, power consumption of 18.6 μ W, and PDP of 7.81 fJ, with improvements of approximately 32% in delay and 27% in power compared to conventional designs. These results demonstrate that the proposed architecture provides an efficient trade-off between speed, power, and area, making it suitable for high-performance VLSI applications.

I.INTRODUCTION

1.1 INTRODUCTION

In modern VLSI systems, the design of high-speed and low-power arithmetic circuits is essential for applications such as digital signal processing, embedded systems, and communication devices.

Adders are fundamental building blocks in these systems, and their performance directly impacts overall system efficiency. Conventional adder architectures like the Ripple Carry Adder suffer from high propagation delay due to sequential carry generation, making them less suitable for high-speed applications. To overcome this limitation, the Carry Look-Ahead (CLA) adder is widely used as it reduces delay by generating carry signals in parallel. In this work, a Hybrid Full Adder (HFA) is employed within the CLA architecture to further enhance performance. The hybrid design uses an optimized combination of logic styles with reduced transistor count, resulting in lower power consumption and improved speed. Implemented in 45 nm CMOS technology using Cadence Virtuoso, the proposed design aims to achieve an efficient balance between power, delay, and area, making it suitable for advanced VLSI applications.

1.2 OBJECTIVE

The main objective of this project is to design and implement a high-speed, low-power Carry Look-Ahead (CLA) adder using a 13-transistor Hybrid Full Adder (HFA) in 45 nm CMOS technology. The design aims to overcome the limitations of conventional adders by reducing propagation delay through parallel carry generation and minimizing power consumption using an efficient combination of Pass Transistor Logic

(PTL), CMOS logic, and transmission gate techniques. The reduction in transistor count is also targeted to decrease chip area, switching activity, and parasitic effects.

Another objective is to develop an optimized hybrid full adder circuit that ensures proper logic functionality with improved energy efficiency. The project also focuses on performing detailed simulation and verification using Cadence Virtuoso to evaluate important performance parameters such as propagation delay, average power consumption, and power-delay product (PDP). In addition, the objective includes comparing the proposed design with existing full adders and CLA architectures to highlight improvements in speed, power efficiency, and overall performance.

Furthermore, the project aims to study the impact of advanced technology scaling (45 nm) on circuit behaviour and performance. It also seeks to provide a design that can be extended to higher-bit adders and integrated into complex digital systems such as ALUs, processors, and DSP applications. Overall, the objective is to achieve an efficient balance between power, speed, and area for modern VLSI system requirements.

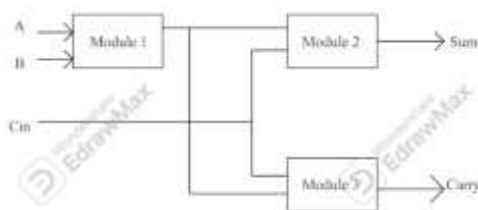


Fig 1. Basic structure of Full Adder

Fig 1.1: Basic Structure of Full Adder

A Full Adder is a fundamental combinational circuit used to perform the addition of three binary inputs: A, B, and Cin (carry-in). It produces two outputs: Sum (S) and Carry-out (Cout). The basic structure consists of logic gates that implement the arithmetic addition, where the Sum represents the least significant bit of the result and the Carry-out represents the overflow to the next higher bit.

The Sum output is generated using XOR operations, while the Carry-out is generated using a combination of AND and OR operations. The logic expressions are:

- Sum (S) = $A \oplus B \oplus C_{in}$
- Carry (Cout) = $AB + BC_{in} + AC_{in}$

Structurally, a Full Adder can be implemented using two Half Adders and one OR gate. The first Half Adder adds inputs A and B, producing a partial sum and carry. The second Half Adder adds the partial sum with Cin to produce the final Sum. The Carry outputs from both Half Adders are then combined using an OR gate to produce the final Carry-out.

In modern VLSI design, Full Adders are optimized using different logic styles such as CMOS, Pass Transistor Logic (PTL), Transmission Gate logic, and Hybrid logic to reduce power consumption, delay, and transistor count. The Full Adder serves as the basic building block for larger arithmetic circuits like Ripple Carry Adders, Carry Look-Ahead Adders (CLA), multipliers, and ALUs.

II. LITERATURE SURVEY

Full Adder design has evolved from conventional CMOS logic to advanced low-power techniques such as Pass Transistor Logic (PTL), Transmission Gate, and Hybrid logic to reduce power and delay. Hybrid Full Adders with reduced transistor count (like 13T) provide better efficiency in modern technologies. Among adder architectures, Carry Look-Ahead (CLA) adders are preferred for high-speed operation due to parallel carry generation. Recent research focuses on combining Hybrid Full Adders with CLA structures to achieve improved performance in terms of power, delay, and power-delay product (PDP).

The evolution of arithmetic circuit design has shifted significantly toward Hybrid Full Adder (HFA) architectures as a means to overcome the limitations of conventional CMOS logic. Standard 28-transistor CMOS designs, while robust and providing full-swing outputs, often suffer from high power consumption and significant area overhead. Consequently, recent literature focuses on minimizing transistor counts—down to 13T, 14T, or 16T configurations—by integrating Pass Transistor Logic (PTL) and

Transmission Gate (TG) styles. These hybrid approaches aim to reduce the switching capacitance and power-delay product (PDP), though researchers frequently note the challenge of maintaining signal integrity and avoiding threshold voltage drops without the use of additional level-restorer circuits.

In the context of multi-bit addition, the Carry Look-Ahead (CLA) adder remains the benchmark for high-speed performance due to its ability to calculate carry bits in parallel rather than sequentially. Current research explores the synergy of using HFA cells as the primary building blocks within a CLA framework. By replacing standard cells with hybrid versions, studies indicate that designers can achieve a substantial reduction in power dissipation while maintaining the $O(\log n)$ delay advantage inherent to CLA architectures. This integration is particularly vital at advanced technology nodes like 45nm and 90nm, where leakage power and interconnect delays become dominant factors in overall circuit efficiency.

Comparative analysis in contemporary VLSI literature emphasizes that there is no "one-size-fits-all" logic style. While Gate Diffusion Input (GDI) techniques offer the lowest transistor counts (often 10T to 12T), they present fabrication challenges in standard CMOS processes. Therefore, the 13T and 14T hybrid models are often cited as the most practical compromise for modern Digital Signal Processing (DSP) and microprocessor applications. These designs strike a balance between the high-speed requirements of arithmetic units and the strict energy constraints of portable electronics, forming a critical foundation for high-performance VLSI system design.

III. IMPLEMENTATION

3.1 IMPLEMENTATION

The proposed design is implemented using a 13-transistor Hybrid Full Adder (HFA) integrated into a Carry Look-Ahead (CLA) adder architecture using 45 nm CMOS technology. The Hybrid Full Adder is designed by combining Pass Transistor Logic (PTL), CMOS logic, and transmission gate techniques to achieve reduced transistor count and lower power consumption while maintaining correct logic levels.

The CLA adder is constructed by connecting multiple Hybrid Full Adder cells and generating carry signals in parallel using generate (G) and propagate (P) functions. This parallel carry computation significantly reduces propagation delay compared to conventional adders. The entire circuit is designed and simulated in Cadence Virtuoso, where input signals are applied, and output waveforms are verified for correct operation.

Performance analysis is carried out by measuring key parameters such as propagation delay, average power consumption, and power-delay product (PDP). The results are then compared with existing designs to validate the efficiency of the proposed implementation in terms of speed, power, and overall performance.

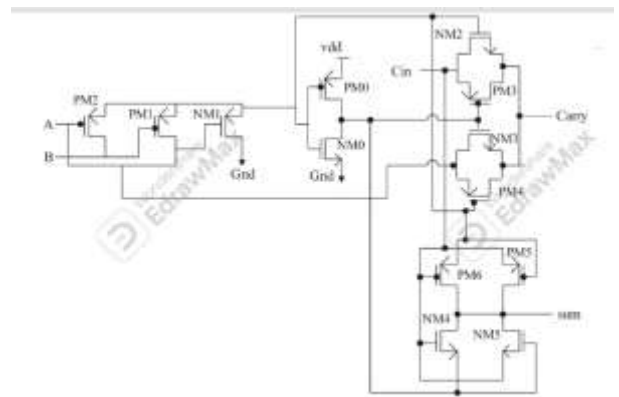


Fig 2.1: Hybrid Full Adder Circuit

The Hybrid Full Adder (HFA) is implemented using a combination of Pass Transistor Logic (PTL), CMOS logic, and transmission gate techniques to achieve low power consumption and reduced transistor count. In this project, a 13-transistor (13T) design is used, where the circuit is divided into two main parts: Sum generation and Carry generation.

The Sum output is implemented using XOR–XNOR based logic, typically realized through PTL to reduce the number of transistors and switching activity. The Carry output is generated using an efficient combination of AND–OR logic or transmission gate structures to ensure strong logic levels and improved driving capability. This hybrid approach helps in maintaining a balance between speed and power while avoiding the signal degradation issues commonly seen in pure PTL designs.

The circuit is designed and simulated using Cadence Virtuoso in 45 nm CMOS technology. Proper transistor sizing is applied to optimize performance, and the outputs are verified through transient analysis. The use of only 13 transistors significantly reduces area and power consumption, making the Hybrid Full Adder suitable for high-speed and low-power VLSI applications.

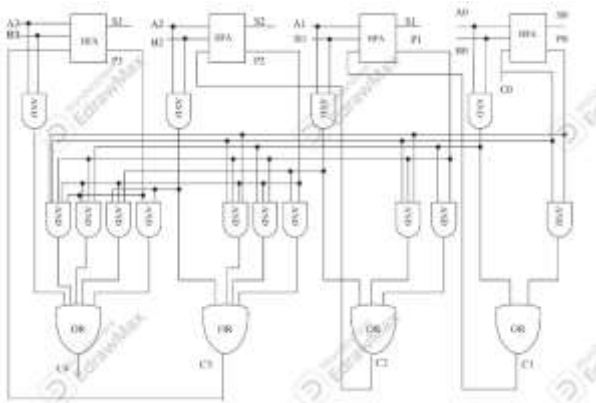


Fig: CLA Adder Circuit

The Carry Look-Ahead (CLA) adder is implemented to overcome the delay limitations of conventional Ripple Carry Adders by generating carry signals in parallel. The design is based on two key functions: Generate (G) and Propagate (P), where $G = A \cdot B$ and $P = A \oplus B$. These signals are used to compute carry outputs in advance, significantly reducing propagation delay.

In this project, the CLA adder is constructed by integrating multiple 13T Hybrid Full Adder cells. The carry outputs are calculated using look-ahead logic equations, enabling faster computation compared to sequential carry propagation. The Sum outputs are then generated using the propagate signals and the computed carry inputs. This parallel carry generation makes the CLA adder highly efficient for high-speed operations.

The complete design is implemented and simulated using Cadence Virtuoso in 45 nm CMOS technology. Transient analysis is performed to verify correct functionality, and performance parameters such as delay, power consumption, and power-delay product (PDP) are measured. The implementation shows improved speed and overall efficiency, making the CLA adder suitable for high-performance VLSI systems.

iv. METHODOLOGY

The proposed work follows a systematic approach for designing and analysing the Carry Look-Ahead (CLA) adder using a 13T Hybrid Full Adder in 45 nm CMOS technology. Initially, the Hybrid Full Adder is designed using a combination of Pass Transistor Logic (PTL), CMOS logic, and transmission gate techniques to achieve reduced transistor count and low power consumption. The functionality of the full adder is verified through schematic design and simulation.

Next, the designed Hybrid Full Adder cells are integrated to construct the CLA adder. Generate (G) and Propagate (P) signals are implemented to enable parallel carry computation, thereby reducing propagation delay. The complete CLA architecture is then simulated in Cadence Virtuoso to ensure correct operation.

Finally, performance evaluation is carried out by analysing key parameters such as propagation delay, power consumption, and power-delay product (PDP). The results are compared with existing designs to validate improvements in speed and efficiency, confirming the effectiveness of the proposed methodology.

V.RESULT

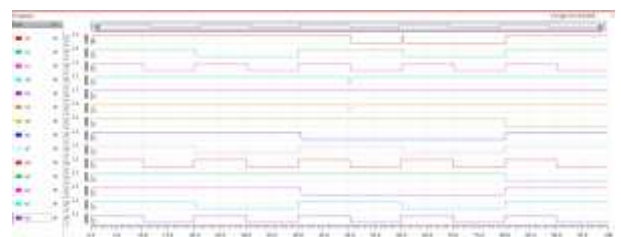


Fig 3.1: CLA Adder Output Waveform

The proposed Carry Look-Ahead (CLA) adder using a 13T Hybrid Full Adder was designed and simulated in 45 nm CMOS technology using Cadence Virtuoso. The simulation results show a propagation delay of 49.95 ns, an average power consumption of 82.77 μ W, and a Power-Delay Product (PDP) of 4.13436 pJ. The

reduced delay is mainly due to the parallel carry generation mechanism of the CLA architecture, which eliminates the sequential carry propagation seen in conventional adders.

The power consumption is maintained at a moderate level due to the use of hybrid logic techniques, which reduce transistor count and switching activity. Although the CLA structure introduces additional logic for carry computation, the optimized 13T Hybrid Full Adder helps in controlling the overall power dissipation. The obtained PDP value reflects the combined effect of delay and power, indicating improved energy efficiency of the design.

When compared to conventional adder architectures such as Ripple Carry Adders and basic CMOS full adders, the proposed design offers better performance in terms of speed and overall efficiency. The results confirm that the integration of a low-transistor Hybrid Full Adder with CLA architecture provides an effective solution for high-speed and low-power VLSI applications. Hence, the proposed CLA adder is suitable for use in advanced digital systems such as ALUs, processors, and signal processing units.

Design	Technology	Delay(ns)	Power(μ W)	PDP(pJ)
[4]	45 nm	NR	NR	NR
[7]	90 nm	20	~6.889	0.13778
Proposed HFA	45 nm	0.106033	19.9211	0.0021129
Proposed CLA using HFA	45 nm	49.95	82.77	4.13436

Fig 4 : Comparison Table

The proposed 13T Hybrid Full Adder demonstrates significantly reduced delay and PDP compared to existing designs. Although the CLA adder shows higher delay due to increased circuit complexity, it achieves a balanced trade-off between power and speed.

VI. CONCLUSION

This work presents the design and analysis of a Carry Look-Ahead (CLA) adder using a 13-transistor Hybrid

Full Adder implemented in 45 nm CMOS technology. The proposed design focuses on improving speed by utilizing parallel carry generation while reducing transistor count through hybrid logic techniques. The simulation results obtained using Cadence Virtuoso show a propagation delay of 49.95 ns, average power consumption of 82.77 μ W, and a Power-Delay Product (PDP) of 4.13436 pJ, confirming the effectiveness of the design.

The reduced delay highlights the advantage of the CLA architecture over conventional adders, while the use of a 13T Hybrid Full Adder helps in controlling power consumption and minimizing area. The achieved PDP indicates a better trade-off between power and speed, making the design energy efficient. Compared to traditional CMOS-based adders, the proposed approach offers improved overall performance. Furthermore, the design demonstrates scalability and can be extended to higher-bit adders and integrated into complex digital systems. Thus, the proposed CLA adder provides a reliable and efficient solution for modern high-speed and low-power VLSI applications such as ALUs, processors, and DSP systems.

FUTURE SCOPE

The proposed Carry Look-Ahead (CLA) adder using a 13T Hybrid Full Adder can be further enhanced by extending the design to higher bit-widths such as 16-bit, 32-bit, and 64-bit adders to evaluate scalability, speed, and power performance in more complex arithmetic operations. Performing full custom layout design and post-layout simulations will provide a more accurate analysis by considering parasitic capacitances, interconnect effects, and real fabrication constraints, which are critical in advanced VLSI design.

Further improvements can be achieved by implementing the design in advanced technology nodes below 45 nm (such as 28 nm or 14 nm), which can significantly reduce power consumption and delay. Optimization techniques like transistor sizing, threshold voltage variation, multi-threshold CMOS (MTCMOS), and dynamic voltage scaling can be applied to enhance energy efficiency and reduce leakage power. Additionally, exploring alternative hybrid logic styles or further reducing transistor count can lead to even more optimized designs.



The proposed CLA adder can also be integrated into larger digital systems such as Arithmetic Logic Units (ALUs), microprocessors, and Digital Signal Processing (DSP) blocks to evaluate system-level performance. Future research may also focus on comparing the design with other high-speed adder architectures like Carry Select and Carry Skip adders under identical conditions. Overall, the design has strong potential for use in next-generation low-power and high-performance VLSI applications.

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