International Journal of Science, Strategic Management and Technology
Volume **02** Issue **05** May-**2026** | ISSN: **3108-1762 (Online)** | Impact Factor: 3.8
An International, Peer-Reviewed, Open Access Scholarly Journal Indexed in recognized academic databases

Design of a Low-Power True Single-Phase Clocked Flip-Flop for High-Performance VLSI Systems

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https://doi.org/10.55041/ijsmt.v2i4.650

Cite this Article: Parvathi, B. L. (2026). Design of a Low-Power True Single-Phase Clocked Flip-Flop for High-Performance VLSI Systems. International Journal of Science, Strategic Management and Technology, *02*(05). https://doi.org/10.55041/ijsmt.v2i4.650

Abstract-Flip-flops (FFs) are fundamental sequential elements in digital systems, and their power consumption significantly influences overall system efficiency. This work presents an energy-efficient True Single-Phase Clocked (TSPC) flip-flop designed for high-performance and low-power applications. The proposed design incorporates an input-aware conditional pre-charge mechanism, which activates only when required, thereby reducing unnecessary switching activity and dynamic power consumption. Furthermore, transistor-level optimization and floating node analysis are employed to enhance energy efficiency without incurring substantial area overhead. Post-layout simulation results demonstrate that the proposed flip-flop achieves a power reduction of up to 84.37% compared to a conventional Transmission Gate Flip-Flop (TGFF) at a 1 V supply voltage under 10% switching activity. The power savings further improve to 98.53% under zero data activity conditions. In addition to power efficiency, the design achieves a 17.6% reduction in clock-to-Q delay, making it suitable for high-speed applications. These results highlight the effectiveness of the proposed TSPC flip-flop for next-generation low-power VLSI systems.

Keywords – True Single Phase Clock (TSPC), D-Flip Flop, Transmission Gate Flip Flop (TG-FF), Single-Event Upset (SEU) and Single Event Transient (SET)

I. INTRODUCTION

Advancements in semiconductor technology have significantly improved the performance of modern digital systems. However, power consumption remains a critical challenge, particularly in battery-operated devices and Internet of Things (IoT) applications, where energy efficiency is a primary concern. Flip-flops (FFs), as fundamental building blocks of sequential circuits, contribute substantially to the overall power consumption of digital systems. Therefore, optimizing flip-flop design is essential for enhancing energy efficiency in advanced electronic architectures.

Among various types, the D flip-flop (D-FF) is one of the most widely used sequential elements, serving as a key component in data storage and synchronization. It captures input data at the active clock edge and retains the value until the next clock cycle. D-FFs are also extensively used in timing-critical applications such as Vernier Time-to-Digital Converters (TDCs), where

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precise time interval measurement is required. In such architectures, left-shifting and right-shifting Vernier TDCs utilize negative-edge-triggered (NET) and positive-edge-triggered (PET) D flip-flops, respectively, to detect the alignment between fast and slow signals.

In a left-shifting Vernier TDC, the negative edges of the start and stop signals propagate along delay lines, while in a right-shifting configuration, the positive edges move in the opposite direction. The interaction between these signals determines the precise timing resolution. By integrating both left- and right-shifting delay paths, a bidirectional Vernier structure can be achieved, enabling improved accuracy and enhanced timing resolution. This makes optimized flip-flop designs highly desirable for high-precision and low-power timing applications.

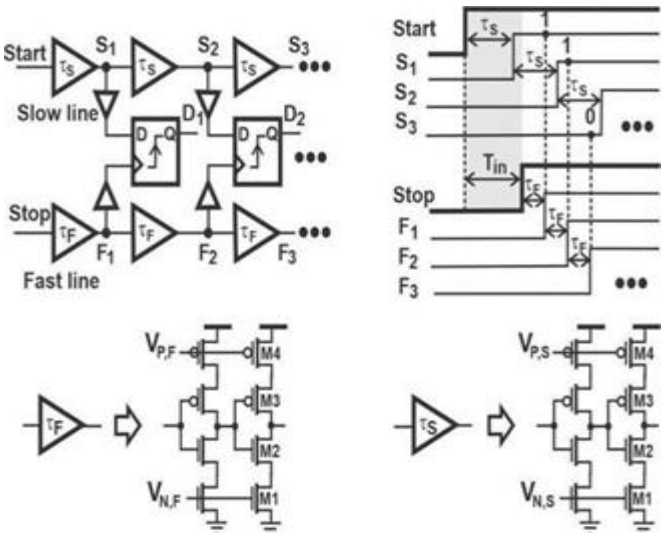

Fig. 1. Vernier TDC with Right-Shifted Configuration

II. D FLIP-FLOP ARCHITECTURES FOR TDCS

D flip-flops (D-FFs) can be broadly classified into three categories: sense-amplifier-based (SA) flip-flops, dynamic flip-flops, and static flip-flops. Among static designs, the transmission-gate (TG) master–slave (MS) D flip-flop is one of the most widely used architectures. It operates as a positive-edge-triggered device, ensuring that the output transitions only at the rising edge of the clock, thereby reducing glitches and improving timing reliability. The master–slave configuration consists of two cascaded latches, where data is first captured by the master latch and then transferred to the slave latch, effectively preventing race conditions.

In contrast, dynamic flip-flops rely on pre-charge and evaluation phases to achieve high-speed operation with reduced transistor count, making them suitable for performance-critical applications. Sense-amplifier-based (SA) flip-flops further enhance speed and energy efficiency by employing a differential sensing mechanism for rapid decision-making. Due to their fast operation and low power characteristics, SA-based designs are widely adopted in high-performance and low-voltage applications.

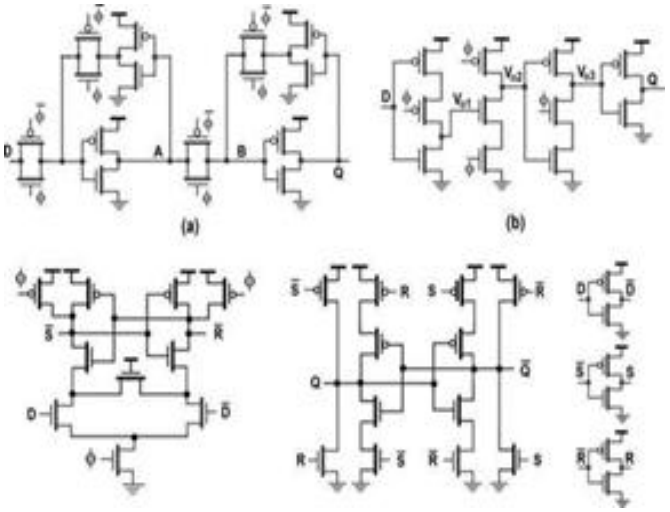

Fig. 2. (a) TG Master-SlaveD-FF,(b) Positive-Edge-Triggered TSPC D-FF, (c) SA D-FF

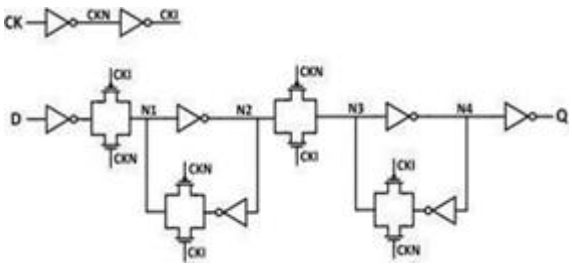

Fig. 3. Schematic of TG-FF

The transmission-gate flip-flop (TGFF) is one of the most widely used flip-flop architectures in modern digital systems due to its robust operation and reliability. It performs effectively even under near-threshold voltage conditions and is inherently contention-free. However, the primary drawback of the TGFF lies in its extensive clock network, which results in significant clock switching power. In addition, several internal nodes toggle regardless of input activity, leading to unnecessary power dissipation even when data transitions are minimal.

To address these limitations, optimizing the usage of clock signals and reducing redundant switching activity are essential. Prior research has introduced several single-phase, low-power flip-flop designs aimed at minimizing clock power. Nevertheless, these designs

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often suffer from issues such as excessive pre-charge power consumption or degraded performance at low supply voltages.

To overcome these challenges, a True Single-Phase Clocked (TSPC) flip-flop architecture is proposed. The design eliminates redundant pre-charge operations through an input-aware mechanism, thereby significantly reducing dynamic power consumption. Furthermore, the proposed flip-flop operates reliably across a wide range of supply voltages without contention, making it a suitable candidate for energy-efficient and high-performance VLSI applications.

III. STUCTURE OF THE TSPCFF

Switch from top to low: During the low phase of the clock (CK = 0), the internal nodes of the flip-flop undergo pre-charge and evaluation preparation. Node N1 is charged to VDD through transistors M11 and M12, while node N2 is also pre-charged to VDD via M6 and M2. At the same time, node N3 is discharged to ground through transistors M9 and M10, resulting in the output Q remaining at logic high. As the clock transitions, node N2 begins to discharge toward ground through transistors M17 and M18, depending on the input condition.

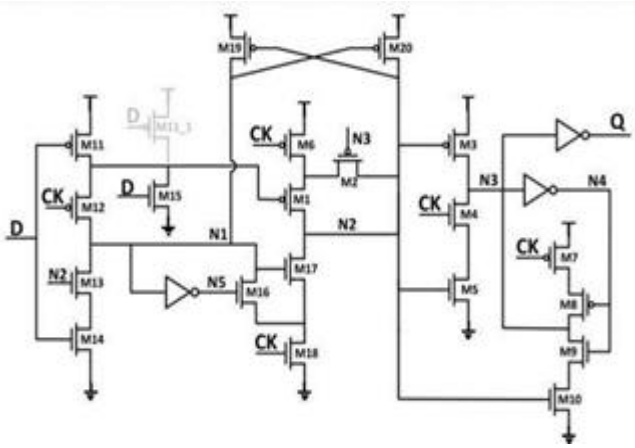

Fig. 4. Schematic of TSPC FF.

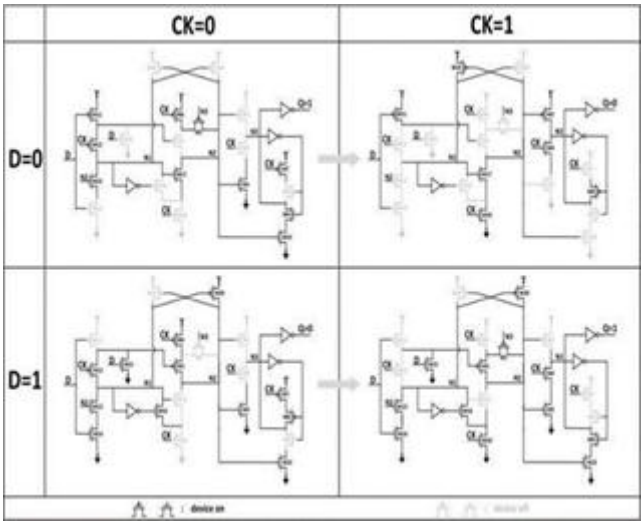

Fig. 5. Operation Diagram of the Proposed FF at Different D and CK.

During this period, transistor M13 turns OFF, effectively isolating the flip-flop from input data variations and preventing unnecessary switching activity. Simultaneously, node N3 is pulled up to VDD through transistor M3, which causes the output Q to transition from high to low (logic 1 → 0). Throughout this half-cycle of the clock, node N1 remains at a high potential, maintained by transistor M19, while node N2 stays near ground due to the conduction path through M17 and M18.

Convert low to high: During the low phase of the clock (CK = 0), node N3 is maintained at a high potential through transistors M7 and M8, keeping the output Q at logic low. Meanwhile, node N2 is pre-charged to VDD via transistors M6 and M1, while node N1 is discharged to ground through M13 and M14. As the clock transitions to the rising edge (CK ↑), transistor M12 turns OFF, isolating the input from the internal nodes and preventing unwanted switching. At the same time, node N3 is discharged to ground through transistors M4 and M5, which triggers the output Q to transition from low to high (logic 0 → 1). During the subsequent half-cycle of the clock, node N1 remains at a low potential due to the conduction path through M16 and M18, while node N2 maintains a stable high voltage level. This stable condition persists until transistor M20 activates, ensuring proper state retention and reliable operation of the flip-flop.

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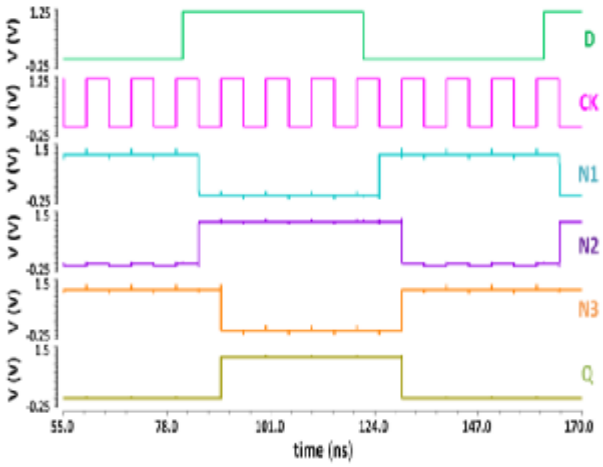

Fig. 6. Time-Domain Signal Representation of TSPC FF

As illustrated in Fig. 7, the capacitance at node N1 is not actively utilized during the SET operation, and N1 is discharged to ground through transistor M22. When the control signal SN is at a low level and SET is asserted high, node N2 is charged to VDD through transistor M20, while the potential at node N1 remains low. Simultaneously, transistor M23 isolates node N3 from the stacked path, and node N3 is discharged through transistor M24. This controlled discharge mechanism ensures efficient switching while maintaining low power consumption.

Fig. 8 presents the transient response of the proposed flip-flop incorporating the SET functionality. When SN = 0, the output Q is forced to a high state, indicating that the flip-flop is initialized or set. Conversely, when SN = 1, the flip-flop resumes normal operation, responding to the clock and input data.

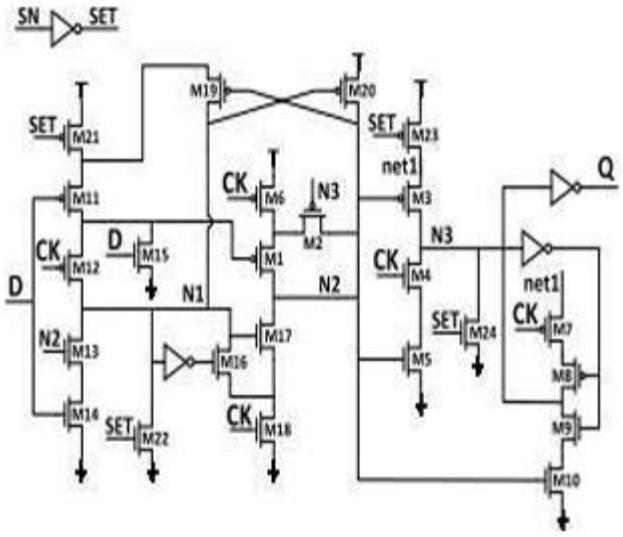

Fig. 7. Schematic of TSPC FF with Set

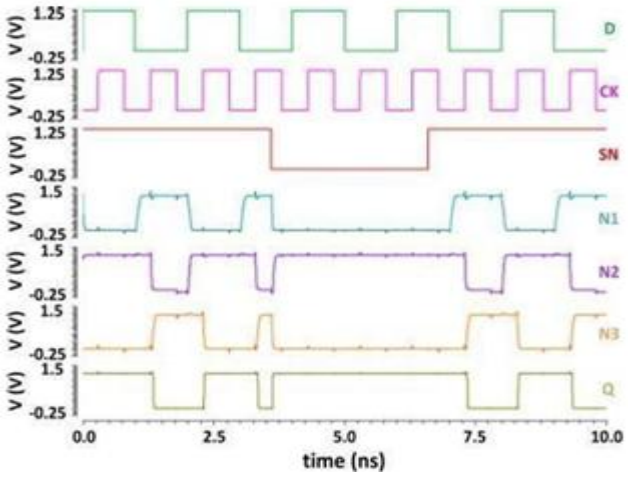

Fig. 8. Time-Domain Signal Representation of TS-PC FF with Set

The schematic of the proposed TSPC flip-flop with SET/RESET functionality is illustrated in the corresponding figure. During the **reset operation**, when the reset signal (**RSTN** or **rtbar**) is asserted low, transistor **M21** disables the charging path of node **N2**, while **M22** actively discharges node **N2** to ground. As a result, node **N2** remains at a low potential. Due to the low voltage at **N2**, node **N3** is charged to VDD through the conduction path of transistor **M3**, which forces the output **Q** to remain at logic low. Simultaneously, transistor **M19** charges node **N1** to a high potential, ensuring proper internal node initialization during the reset phase. To further enhance robustness, when **CK = 0** and **D = 1**, an additional PMOS transistor (**M23**) is introduced to isolate node **N1** from the input. This prevents direct current paths between transistors (such as M12 and M15), thereby eliminating short-circuit power dissipation. Fig. 9 illustrates the transient response of the proposed flip-flop under reset conditions. When **RSTN** is held low, the output **Q** remains at logic 0, indicating that the flip-flop is in the reset state. When **RSTN** transitions to a high logic level, the flip-flop resumes normal operation and correctly captures input data on the active clock edge.

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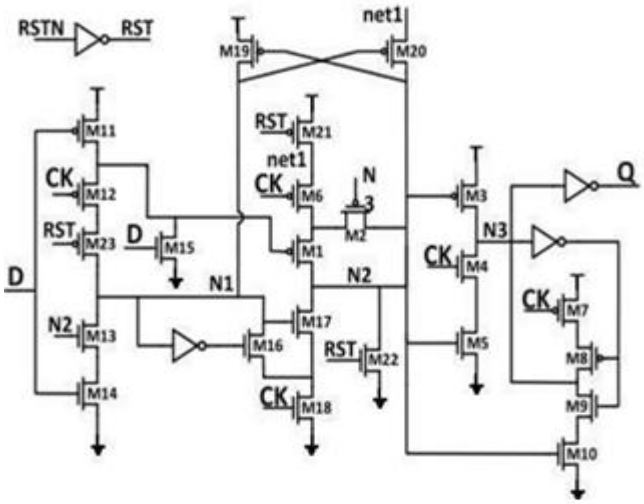

Fig. 9. Schematic of TS-PC FF with Reset.

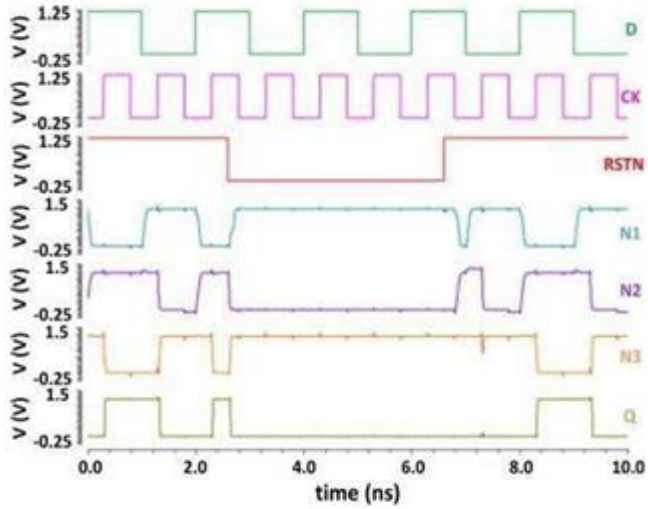

Fig. 10. Time-Domain Signal Representation of TS-PC FF with Reset.

Transient Error–Tolerant Enhancement of the Proposed Flip-Flop:

Aggressive voltage scaling is an effective approach to reduce power consumption in modern digital systems; however, it significantly increases susceptibility to soft errors such as Single Event Upsets (SEUs) and Single Event Transients (SETs). To ensure reliable operation under low-voltage conditions, the proposed flip-flop (FF) is enhanced with transient error tolerant features. As illustrated in Fig. 9, node N2 is particularly sensitive to SEU-induced disturbances, where a sudden discharge from VDD to ground can corrupt the stored data. This disturbance may inadvertently activate transistors such as M3 and M19, leading to unintended charging of internal nodes N1 and N3, thereby propagating errors to the output. To mitigate this issue, a C-element-based hardening technique is incorporated into the design, as shown in Fig. 10. The enhanced architecture introduces isolation between critical nodes using control transistors governed by signal N2R. As a result, even if node N2 is affected by an SEU, nodes N1 and N3 remain electrically isolated and retain their original states. This prevents erroneous switching and ensures output stability. Consequently, the proposed SEU-tolerant flip-flop significantly improves robustness against transient faults while maintaining energy efficiency and high-performance operation.

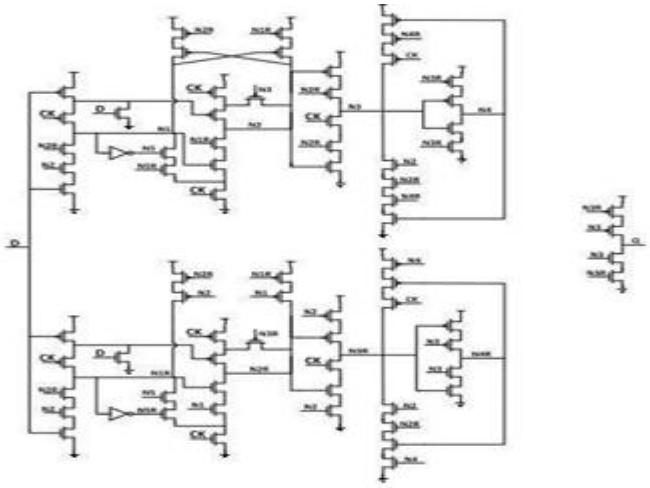

Fig. 11. Schematic of SEU tolerant

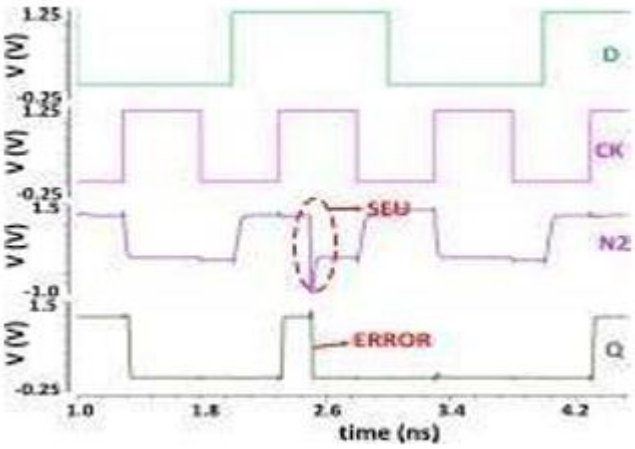

Fig. 12. Time-domain signal representation of a Single Event Upset (SEU) at the locus of node N2

IV. RESULTS AND DISCUSSIONS

The proposed flip-flop (FF) demonstrates superior performance compared to the conventional Transmission Gate Flip-Flop (TGFF), achieving approximately 4.8% improvement in overall efficiency, making it well-suited for large-scale integrated circuit applications. A key advantage of the design is the elimination of redundant

pre-charge operations, which significantly enhances energy efficiency. Under minimal data activity conditions, the proposed FF consumes only 1.5% of the power dissipated by TGFF, as it primarily incurs leakage power while avoiding unnecessary internal switching. In contrast, TGFF continues toggling internal nodes (such as CKN and CKI), resulting in higher power consumption.

Across a range of supply voltages, the proposed FF achieves over 80% power savings compared to TGFF, along with a 17.5% reduction in clock-to-Q delay at 1 V, enabling high-speed operation. However, the setup time is slightly increased due to the data-dependent pre-charge mechanism involving multiple transistors. The hold time remains negligible, comparable to TGFF. Variants with reset and scan functionalities introduce minor delay and setup overheads due to additional capacitance and weakened pull-down paths. Furthermore, the SEU-tolerant version exhibits increased delay due to C-element integration, with a slight setup time penalty.

TABLE 1. COMPARATOR BETWEEN TGFF AND TSPC

Parameters	**TGFF Conventional**	**TSPC**
Single-Phase clocked	NO	YES
Low voltage operation	YES	YES
Power (nW)	3.69µW	2.02µW
Setup Time	18	92
Hold Time	0	1
Delay (clk-to-Q) (ps)	20.0173n	17.5091n

V. CONCLUSION

This paper presents an energy-efficient True Single-Phase Clocked flip-flop (TSPC FF) designed to reduce power consumption while maintaining high performance. The proposed design minimizes unnecessary switching activity through an input-aware mechanism and eliminates redundant pre-charge operations. In addition, floating node analysis is employed to prevent short-circuit paths, thereby improving reliability and reducing dynamic power dissipation. Further optimization at the transistor level contributes to both power and area efficiency.

Post-layout simulation results demonstrate that, under data activity below 10%, the proposed flip-flop achieves approximately 80% lower power consumption compared to the conventional Transmission Gate Flip-Flop (TGFF). Experimental validation from test chip measurements further confirms the superior energy efficiency of the design. Moreover, the proposed flip-flop achieves a 17.5% reduction in clock-to-Q delay, enhancing its suitability for high-speed applications. These improvements are achieved with minimal area overhead, as the proposed design occupies only 4.8% more area than TGFF. Overall, the proposed TSPC FF offers an effective trade-off between power, speed, and area for modern low-power VLSI systems..

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