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Low Power 8-Bit Alu Design using M-GDI Technique

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ABSTRACT

This paper presents the design and implementation of an 8-bit Arithmetic Logic Unit (ALU) using Modified Gate Diffusion Input (M-GDI) technique. The proposed design focuses on reducing power consumption, propagation delay, and area compared to conventional CMOS logic. The ALU performs multiple operations such as **AND, OR, XOR, NAND, NOR, NOT**, addition, and subtraction using an efficient 8:1 multiplexer structure. The design is implemented and simulated using Cadence tools. The design is implemented and simulated using **Cadence** tool. Results show that the M-GDI based ALU achieves significant improvement in speed and power efficiency, making it suitable for modern VLSI applications. The ALU is developed and simulated using Cadence Design Systems with the 45 GDK (Generic Design Kit)**.**

Keywords:

ALU, M-GDI Technique, VLSI, Low Power Design, Multiplexer, Cadence.

INTRODUCTION

In this project, an 8-bit ALU is designed and implemented using the M-GDI technique to achieve optimized performance in terms of speed, power, and area. The design incorporates various logic gates and arithmetic circuits such as adders and multiplexers using M-GDI cells, ensuring efficient operation with minimal hardware complexity.

To overcome these limitations, the Modified Gate Diffusion Input (M-GDI) technique has emerged as an efficient design methodology in VLSI systems. The M-GDI technique is an improved version of the basic Gate Diffusion Input (GDI) method, offering significant reduction in power consumption, propagation delay, and transistor count while maintaining better logic functionality. By using fewer transistors compared to traditional CMOS logic, M-GDI enables compact circuit design with enhanced performance, making it highly suitable for low-power application.

The proposed design is simulated and verified using Cadence Virtuoso. Cadence provides a robust environment for schematic design, simulation, and performance analysis, enabling accurate evaluation of circuit parameters such as power consumption, delay, and functionality.

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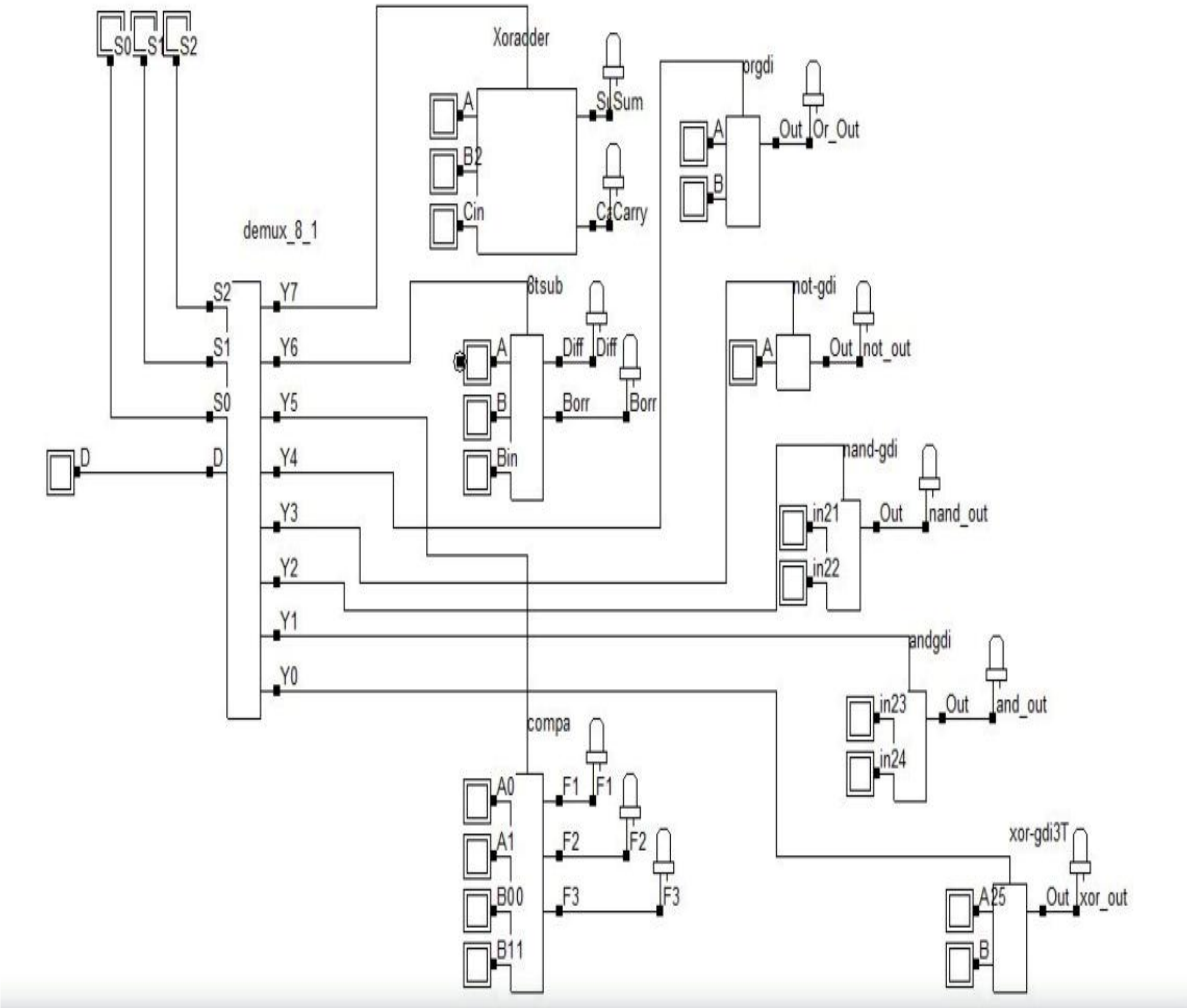
EXISTING METHOD

The existing method for designing an 8-bit Arithmetic Logic Unit (ALU) using conventional techniques is typically implemented using 180 nm CMOS technology and simulated or verified using Xilinx software tools. The 180 nm technology node is widely used in earlier VLSI designs due to its stability, ease of fabrication, and well-established design rules. However, it results in higher power consumption, larger chip area, and slower switching speed compared to more advanced technologies. The existing method serves as a baseline design approach for 8-bit ALUs, focusing more on functionality and ease of implementation rather than optimization.



PROPOSED METHOD

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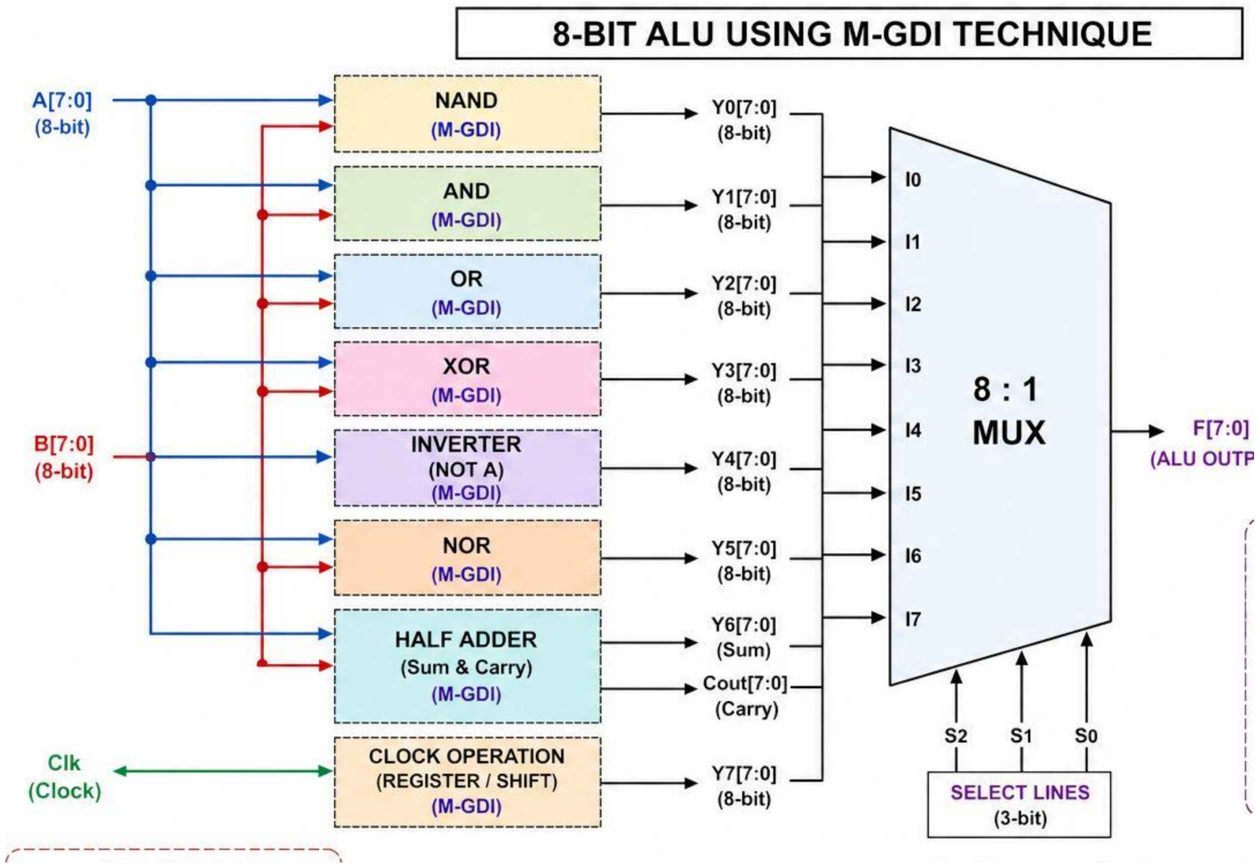

The proposed method for designing an 8-bit Arithmetic Logic Unit (ALU) focuses on the use of the Modified Gate Diffusion Input (M-GDI) technique implemented in 45 nm CMOS technology using Cadence tools. The use of Cadence software plays a crucial role in the proposed methodology. It provides a comprehensive environment for schematic design, simulation, layout creation, and verification at the transistor level. Unlike conventional CMOS logic, the M-GDI technique significantly reduces the number of transistors required to implement basic logic gates, thereby minimizing power consumption, propagation delay, and chip area. The use of 45nm technology further enhances the performance by enabling faster switching speeds, lower threshold voltages, and reduced parasitic capacitances, making the design highly efficient for modern VLSI applications.

METHODOLOGY

The ALU is designed to perform a set of arithmetic and logical operations such as addition, subtraction, AND, OR, XOR, and NOT. Based on these requirements, a block-level architecture of the ALU is developed, where the overall system is divided into smaller modules like logic unit, arithmetic unit, and control unit. Each module is designed to handle specific operations, and a multiplexer is used to select the required output based on control signals. After designing individual components, the next phase is integration, where all modules are combined to form the complete 8-bit ALU. Multiplexers are used extensively to switch between arithmetic and logic outputs.

The design is then implemented at the transistor level using Cadence tools, which provide a platform for schematic entry, simulation, and verification. Simulation and verification form a critical part of the methodology. Functional simulation is performed to verify that the ALU produces correct outputs for all possible input combinations. Timing analysis is also carried out to evaluate the propagation delay and ensure that the design meets speed requirements. Power analysis is conducted to confirm the reduction in power consumption achieved through the M-GDI technique.

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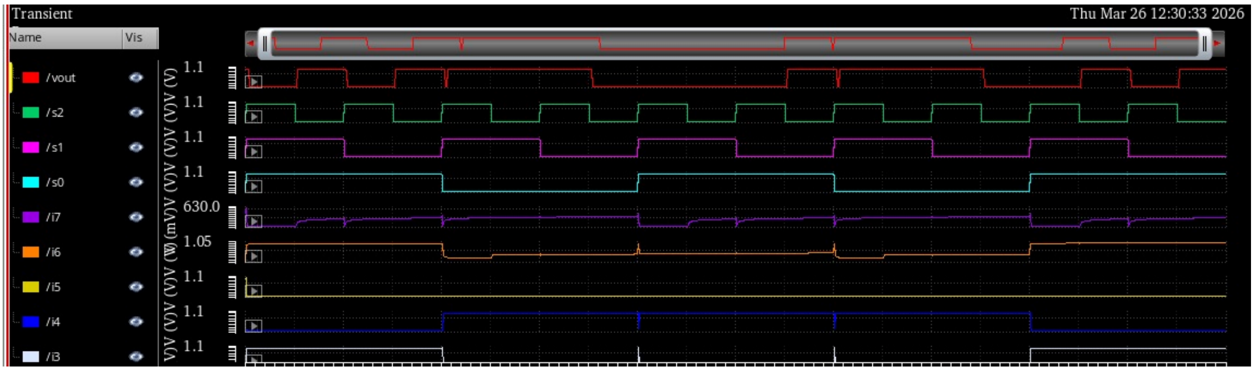
RESULT



The implemented 8-bit ALU using M-GDI shows:
Performance Improvements.
Reduced power consumption.
Lower propagation delay.
Reduced transistor count.
Smaller chip area.

CONCLUSION

This paper presents the design and implementation of an efficient 8-bit ALU using the M-GDI technique. The proposed design significantly reduces power consumption, delay, and transistor count compared to traditional CMOS-based ALUs. The use of Cadence Virtuoso ensures accurate simulation and verification of the design.The results confirm that the M-GDI technique is highly suitable for low-power and high-speed VLSI applications, making it an effective solution for modern digital systems**.** The project on 8-bit ALU design using M-GDI technique successfully demonstrates the design, simulation, and analysis of a low-power, high-speed arithmetic and logic unit. By employing the Modified Gate Diffusion Input (M-GDI) technique, the ALU achieves reduced transistor count, lower power consumption, and faster propagation delay compared to conventional CMOS-based designs.

FUTURE SCOPE

The proposed 8-bit ALU design using the Modified Gate Diffusion Input (M-GDI) technique demonstrates significant improvements in power efficiency, speed, and area reduction. However, there are several opportunities for further enhancement and extension of this work.

One of the major future directions is the extension of the current design to higher bit-width architectures such as 16-bit, 32-bit, or 64-bit ALUs. This would make the design more suitable for advanced processors and high-performance computing systems challenge.

Another potential improvement lies in integrating the ALU into complete processor architectures. The proposed M-GDI based ALU can be incorporated into microprocessors**,** digital signal processors (DSPs), and embedded systems to evaluate its real-time performance in practical applications.

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