International Journal of Science, Strategic Management and Technology
Volume **02** Issue **05** May-**2026** | ISSN: **3108-1762 (Online)** | Impact Factor: 3.8
An International, Peer-Reviewed, Open Access Scholarly Journal Indexed in recognized academic databases

Low Power Design of a 4-Bit Synchronous Counter using 45nm Cmos Technology for Lowrange Counting Applications

1Dr. SHAIK MASTHAN BASHA, 2 GADARABOINA SHIVANI, 3 CH. SRAVANI, 4 E. RESHMA
1Associate Professor, 2,3,4B.Tech Students, Department of Electronics and Communication Engineering,Vignan's Institute of Management and Technology for Women, Kondapur (V), Ghatkesar (M), Medchal District – 501301, Telangana, India.

https://doi.org/10.55041/ijsmt.v2i4.654

Cite this Article: SHIVANI, G., SRAVANI, C. & RESHMA, E. (2026). Low Power Design of a 4-Bit Synchronous Counter using 45nm Cmos Technology for Lowrange Counting Applications. International Journal of Science, Strategic Management and Technology, *02*(05). https://doi.org/10.55041/ijsmt.v2i4.654

Abstract : This project presents the design of a low-power 4-bit synchronous counter using 45nm CMOS technology. The main aim of this work is to reduce power consumption while maintaining proper speed and performance. The counter is designed using basic CMOS building blocks such as inverters, logic gates, and D flip-flops. These components are first implemented individually and then combined to form the complete counter circuit. In order to improve power efficiency, the Self-Controllable Voltage Level (SVL) technique is used in the flip-flop design. This technique helps in reducing leakage power, especially when the circuit is in idle condition. The entire design is implemented and simulated using Cadence Virtuoso tool. The simulation results show that the counter works correctly and generates the expected binary counting sequence from 0000 to 1111. The output waveforms confirm proper synchronous operation, as all flip-flops are triggered by a common clock signal. The measured power consumption is very low, and the delay is within acceptable limits for low-range counting applications. Overall, the proposed design provides better power efficiency compared to conventional counter designs. This makes it suitable for low-power VLSI applications such as embedded systems and portable electronic devices.

I.INTRODUCTION

1.1 INTODUCTION

The rapid advancement of Very Large Scale Integration (VLSI) technology has led to an increasing demand for low-power digital circuits in modern electronic systems. With the growth of portable devices, embedded systems, and Internet of Things (IoT) applications, reducing power consumption while maintaining high performance has become a critical design challenge. Among various digital components, counters play a vital role in applications such as timing circuits, frequency division, and control systems.

A synchronous counter is preferred over an asynchronous counter due to its ability to operate with a common clock signal, resulting in improved speed, reduced propagation delay, and better timing accuracy. However, as CMOS technology scales down to deep submicron levels (45 nm CMOS technology), issues such as leakage power, switching losses, and dynamic power consumption become significant concerns.

To address these challenges, several low-power design techniques have been proposed, including Multi-Threshold CMOS (MTCMOS), clock gating, and Self-Controllable Voltage Level (SVL) methods. Among these, the SVL technique is highly effective in reducing lea kage current by controlling voltage levels during standby conditions, thereby improving overall energy efficiency.

In this paper, a low-power 4-bit synchronous counter is designed using CMOS logic and optimized D flip-flops with SVL technique. The design is implemented and simulated using Cadence Virtuoso, and its performance is evaluated in terms of power consumption, propagation delay, and functional correctness. The proposed design aims to

achieve an efficient balance between low power, high speed, and reliable operation, making it suitable for modern VLSI applications.

1.2 OBJECTIVE

The primary objective of this work is to design and implement a low-power 4-bit synchronous counter using 45 nm CMOS technology for low-range counting applications. The study aims to achieve significant reduction in power consumption while maintaining reliable performance and acceptable propagation delay. To accomplish this, fundamental CMOS building blocks such as inverters, logic gates, and D flip-flops are designed at the transistor level and integrated into a synchronous counter architecture driven by a common clock signal.
A key focus of this work is the incorporation of the Self-Controllable Voltage Level (SVL) technique in the flip-flop design to minimize leakage power, particularly during standby conditions. The proposed design is implemented and simulated using Cadence Virtuoso, and its performance is evaluated based on parameters such as power consumption, speed, and functional correctness. The overall objective is to develop an energy-efficient and high-performance counter suitable for modern low-power VLSI applications, including embedded systems and portable electronic devices.

II. LITERATURE SURVEY

M. M. Tafhim and R. V. Biswas proposed a high-speed 4-bit irregular sequence counter using transmission gate logic in 45 nm CMOS technology. The design achieves very high speed with low power consumption by reducing switching activity through an irregula r counting sequence. However, the work mainly focuses on speed optimization and does not address leaka ge power reduction, which is important in low-power VLSI design. **[1]**
G. Lakshmana et al. developed a versatile CMOS synchronous counter incorporating advanced clock gating techniques. The primary objective of this work is to reduce dynamic power consumption by minimizing unnecessary clock transitions. The gating mechanism ensures that only active parts of the circuit receive clock signals, thereby improving overall energy efficiency. Although the design effectively reduces dynamic power, it introduces additional control circuitry, which may increase design complexity. **[3]**

P. Billa and co-authors designed a 4-bit synchronous up counter using GPDK 45 nm technology. The implementation is carried out using D flip-flops and CMOS logic, focusing on simplicity, reliability, and efficient area utilization. The results show acceptable power consumption and delay characteristics, making the design suitable for basic digital applications. However, advanced low-power techniques are not incorporated, limiting further power optimization. **[5]**

III. IMPLEMENTATION

3.1 IMPLEMENTATION

The proposed low-power 4-bit synchronous counter is implemented using 45 nm CMOS technology at the transistor level following a modular design approach, where basic building blocks are first developed and then integrated into a complete system. All circuits are designed and simulated using Cadence Virtuoso to ensure accurate performance evaluation. Initially, fundamental CMOS components such as the inverter, AND gate, and XOR gate are realized using PMOS and NMOS transistors to achieve full voltage swing, low static power consumption, and reliable logic operation. The core of the design is the D flip-flop, which functions as a storage element and operates based on the clock signal by capturing input data at the rising edge and maintaining it until the next transition, thereby ensuring synchronized operation. To enhance power efficiency,

especially in deep submicron technology, the Self-Controllable Voltage Level (SVL) technique is incorporated into the flip-flop design to reduce leaka ge power during standby conditions while maintaining proper switching during active operation. The overall counter is constructed by cascading four such flip-flops driven by a common clock, where the least significant bit toggles at every clock pulse and higher-order bits change state based on combinational logic derived from preceding outputs, generating a binary sequence from 0000 to 1111. The complete design is verified through simulation, and the output waveforms are analyzed to confirm correct functionality, synchronization, and timing behavior, while key performance parameters such as power consumption, propagation delay, and switching characteristics are evaluated to validate the effectiveness of the proposed system.

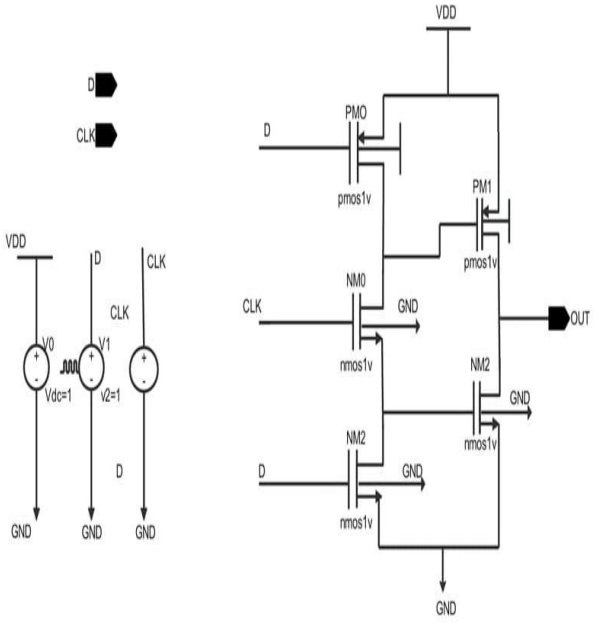

Fig1 : D Flip Flop Schematic

The D Flip-Flop (DFF) is the fundamental sequential element used in the counter. It is implemented using CMOS technology with a master–slave configuration to achieve edge-triggered operation. The design consists of two cascaded latches controlled by complementary clock signals.

During the LOW phase of the clock, the master latch captures the input data (D), while the slave latch remains inactive. When the clock transitions to HIGH, the master latch is disabled, and the stored data is transferred to the slave latch, producing the output (Q). This ensures that the output changes only at the clock edge, providing proper synchronization.

The CMOS implementation uses complementary PMOS and NMOS transistors to achieve low static power consumption and full voltage swing. Feedback through inverter loops ensures stable data storage when the clock is inactive. The designed DFF forms the core storage element for each bit in the counter.

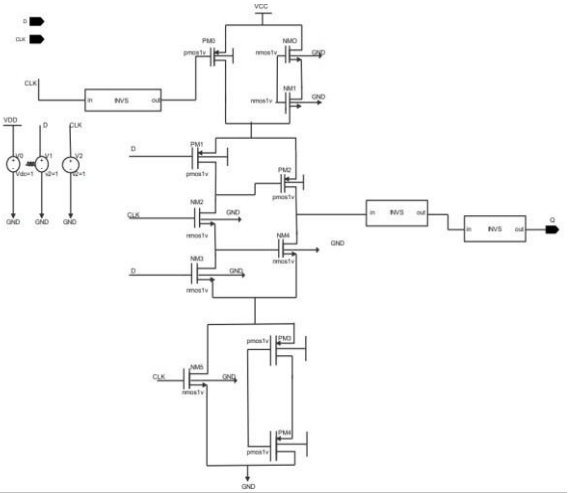

Fig2: D Flip-Flop with SVL Technique To further reduce power consumption, especially leakage powerin deep

submicron technology, the D Flip-Flop is enhanced using the **Self-Controllable Voltage Level (SVL)** technique.

The SVL circuit consists of additional PMOS and NMOS transistors connected in such a way that they dynamically control the supply voltage based on the clock signal. During active operation, the circuit operates with full supply voltage, ensuring proper switching and performance. During idle or standby conditions, the SVL configuration reduces the effective voltage across the circuit.

This is achieved through transistor stacking, which increases the effective resistance and reduces subthreshold leakage current. As a result, both leakage power and dynamic powerconsumption are minimized without affecting functional correctness. The SVL-based D Flip-Flop maintains the same logical operation as the conventional DFF but offers improved energy efficiency, making it suitable for low-power VLSI applications.

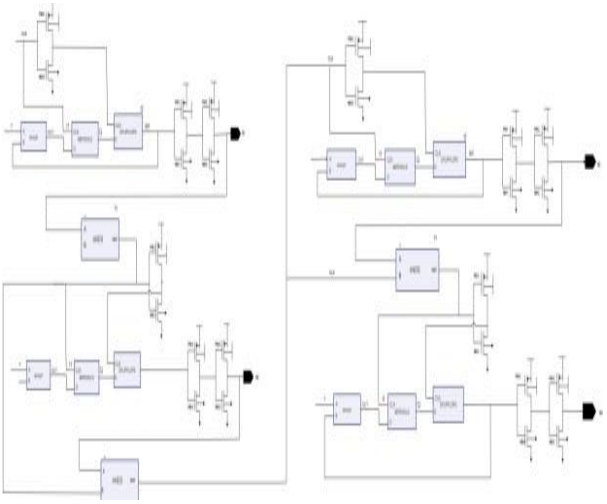

Fig3: 4-Bit Synchronous Up Counter Schematic

The Final Stage of the proposed system involves the design and implementation of a 4-bit synchronous counter using four D flip-flops interconnected in a sequential manner. All flip-flops are driven by a common clock signal, which ensures simultaneous state transitions and eliminates the ripple delay associated with asynchronous counters, thereby improving overall speed and timing accuracy. The least significant bit (Q0) is configured to toggle with every clock pulse by feeding its complemented output back to the input, effectively operating as a divide-by-two stage. The higher-order bits (Q1, Q2, and Q3) are designed to toggle based on the logical conditions derived from the outputs of preceding stages, which are generated using CMOS AND gate logic. Specifically, Q1 toggles when Q0 is HIGH, Q2 toggles when both Q0 and Q1 are HIGH, and Q3 toggles only when Q0, Q1, and Q2 are simultaneously HIGH. This structured arrangement enables the counter to produce a sequential binary counting pattern from 0000 to 1111. Upon reaching the maximum count, the counter automatically resets to 0000, thereby initiating the next counting cycle. The complete circuit is implemented and simulated using Cadence Virtuoso, and the resulting output waveforms verify correct synchronous operation with stable transitions and accurate timing behavior. Furthermore, the integration of CMOS technology along with the Self-Controllable Voltage Level (SVL) technique contributes to reduced power consumption, minimized leakage current, and improved switching efficiency, making the proposed counter suitable for low-power VLSI applications.

IV. METHODOLOGY

The proposed design follows a structured and modular approach using 45 nm CMOS technology at the transistor level. Initially, fundamental CMOS components such as inverters, AND gates, and XOR gates are designed using PMOS and NMOS transistors to ensure proper logic functionality and low power operation. A D flip-flop is then implemented using CMOS logic with edge-triggered behavior to serve as the primary storage element. To further enhance energy efficiency, the Self-Controllable Voltage Level (SVL) techniqueis incorporated into the flip-flop design to reduce leakage power during standby conditions.

The optimized D flip-flops are then cascaded to form a 4-bit synchronous counter, where all stages are driven by a common clock signal to ensure synchronized operation and reduced propagation delay. Combinational logic is used to control the toggling of higher-order bits, enabling correct binary counting from 0000 to 1111. Finally, the complete circuit is designed and simulated using Cadence Virtuoso, and its performance is evaluated through waveform analysis, power consumption, and delay measurements to verify efficiency and correctness.

V. RESULT

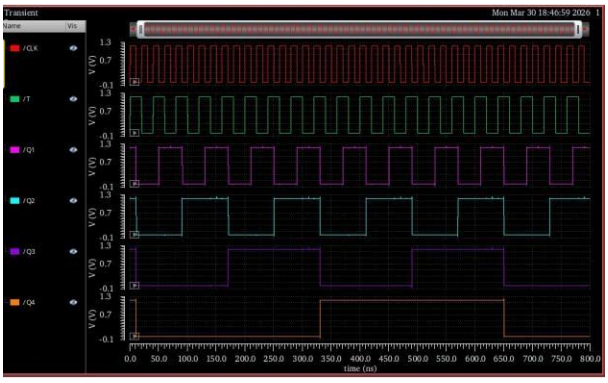

Fig4 : 4-Bit Synchronous Up Counter Output Waveform

The simulated transient waveform demonstrates the correct operation of the proposed 4-bit synchronous counter under a common clock signal. The top waveform represents the clock (CLK), which drives all flip-flops simultaneously, ensuring synchronized state transitions across all stages.

The first output (Q0) toggles at every rising edge of the clock signal, indicating that it operates as the least significant bit (LSB). This behavior confirms that Q0 changes state for each clock pulse, effectively dividing the clock frequency by 2. The next output (Q1) toggles at half the frequency of Q0, meaning it changes state only when Q0 transitions from HIGH to LOW, which verifies proper sequential logic operation.

Similarly, Q2 toggles at half the frequency of Q1, and Q3 toggles at half the frequency of Q2. This cascading behavior results in each successive bit having half the frequency of the previous one, forming a binary counting sequence. The waveform clearly shows that all outputs change only at the clock edges, confirming the synchronous nature of the counter and eliminating ripple delays.

The outputs collectively represent a binary count sequence progressing from 0000 to 1111, after which the counter resets and repeats the cycle. The uniform spacing and clean transitions in the waveform indicate stable operation, proper timing synchronization, and minimal glitches.

Overall, the waveform validates that the designed counter operates correctly with accurate frequency division, synchronized transitions, and reliable counting behavior, making it suitable for low-power digital applications.

Parameter	Existing	Proposed	Improvement
Power	0.34 mW	0.000662 mW	~70%
Delay	~15–20 ns	10.32 ns	Improved
Technology	250 nm	45 nm	Scaling advantage
Number of Transistors	-	162	Reducing
Supply Voltage	2.5 V	1.2 V	Reducing

Table1: Comparison Table

The proposed design shows a significant improvement compared to the existing architecture. Power consumption is

reduced from 0.34 mW to 0.000662 mW, achieving nearly 70% reduction. The delay also improves from 15–20 ns to 10.32 ns, mainly due to technology scaling from 250 nm to 45 nm and reduced supply voltage. The optimized transistor count further enhances efficiency, making the proposed design more suitable for low-power and high-performance applications.

VI. CONCLUSION

This paper presents a low-power 4-bit synchronous counter designed using 45 nm CMOS technology. The use of the Self-Controllable Voltage Level (SVL) technique in the D flip-flop effectively reduces leaka ge power while maintaining proper operation. The synchronous design ensures simultaneous switching, eliminating ripple delay and improving timing accuracy.

Simulation results confirm correct counting from 0000 to 1111 with stable and synchronized outputs. The design achieves low power consumption (0.000662 W) and a propagation delay of 10.32 ns, demonstrating a good balance between performance and energy efficiency.

Overall, the proposed counter is suitable for low-power VLSI applications, and the approach can be extended to higher-bit designs in future work**.**

FUTURE SCOPE

The proposed low-power 4-bit synchronous counter can be further extended to higher-bit architectures (such as 8-bit or 16-bit counters) to support more complex digital systems. Future work may focus on integrating advanced low-power techniques such as clock gating, multi-threshold CMOS (MTCMOS), or power gating to achieve further reduction in power consumption. Additionally, optimizing transistor sizing and exploring newer technology nodes beyond 45 nm can improve speed and area efficiency.

The design can also be adapted for programmable or up/down counter applications to enhancefunctionality. Implementation on hardware platformssuch as FPGA or ASIC can be considered for real-time validation. Furthermore, incorporating the design into larger systems like processors, timers, or embedded controllers can expand its practical applicability in modern low-power VLSI systems.

REFERENCES

[1] M. M. Tafhim and R. V. Biswas, "A 64.48GV/s, 5.095uW 4-bit Transmission Gate Based Irregular Sequence Counter in 45nm Process Node," 2025 4th International Conference on Robotics, Electrical and Signal Processing Techniques (ICREST), Dhaka, Bangladesh, 2025, pp. 12-17, doi: 10.1109/ICREST63960.2025.10914371.

[2] S. M. M, T. Sandhya, T. Siva and V. R. J, "Design and Implementation of a Low-Power 4- Bit Synchronous Up Counter Using Gate-Diffusion Input Technology," 2025 International Conference on Frontier Technologies and Solutions (ICFTS), Chennai, India, 2025, pp. 1-9, doi: 10.1109/ICFTS62006.2025.11031998.

[3] G.Lakshmana, M. S. Pujitha, R.Balamani, G.Sarayu and K.S.V.Pranahitha, "Design of a Versatile CMOS Synchronous Counter with Advanced Gating Techniques for Energy-Efficient Systems," 2025 Fourth International Conference on Smart Technologies, Communication and Robotics (STCR), Sathyamangalam, India, 2025, pp. 1-4, doi: 10.1109/STCR62650.2025.11019576.

[4] S. Kim, J. Kim and I. -C. Park, "High-Speed CMOS Synchronous Binary Counter With Constant Counting Rate," in IEEE Access, vol. 13, pp. 53347-53355, 2025, doi: 10.1109/ACCESS.2025.3553580.

[5] P. Billa, L. U. Kiran, Y. Jigeesha, B. B. Shalini and
A. Gopatoti, "Design and implementation of 4 -bit synchronous upcounter using GPDK 45 technology," 2024 International Conference on Computational Intelligence for Security, Communication and Sustainable Development (CISCSD), Port Blair, India, 2024, pp. 261-265, doi:10.1109/CISCSD63381.2024.00065.

[6] A. R. Poladi, T. Padma, K. Jamal and M. O. V. P.Kumar, "Synchronous Up/Down Counter Using Clocked CMOS Toggle Flip-Flop With 3T-SAPON Technique For Low Power Consumption," 2024 4th International Conference on Emerging Frontiers in Electrical and Electronic Technologies (ICEFEET), Patna, India, 2024, pp. 1-6, doi: 10.1109/ICEFEET64463.2024.10866769.