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Design of High Speed Low Power Processor using FSM-Based Control

Author Details:
Ms. Mansi M Somanache
[1] Department of Electronics and Communication Engineering, VTU, Belagavi, India
Corresponding Author Email: mansisomanache@email.com

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Abstract

The need for faster performance and low power consumption in computer systems is driving the search for better architectures. This paper is the design and implementation of a high-speed low-power 16-bit processor with FSM as a control unit. A Mealy FSM was designed and modified to manage instruction execution across five stages which are fetch, decode, execute, memory access and write back. Combining FSM based control with clock gating proved effective in reducing dynamic power consumption without compromising performance. The processor was modelled in Verilog HDL and synthesized on a Xilinx platform. Functional verification confirmed that all instructions execute correctly. Register values, ALU outputs and Program Counter updates all behaved as expected during simulation.

Power analysis of the on chip design shows a total power consumption of 0.128 W. Dynamic power accounts for 0.106 W of this figure while static leakage power stands at 0.022 W. Timing analysis shows the processor can operate at a maximum frequency of 182 MHz. This is well above the target operating frequency of 68 MHz. These results confirm that the FSM based architecture successfully achieves low power operation while maintaining high speed performance.

Keywords—FSM Controller; Low Power Processor; High-Speed Processor; Verilog HDL; Clock Gating.

I. INTRODUCTION

Modern embedded systems require processors that deliver high computational speed while consuming minimal power. The rapid growth of portable consumer devices, IoT platforms and battery powered systems has made energy efficient processor design more important than ever. Conventional processor architectures often consume excessive dynamic power due to poorly structured control logic that triggers unnecessary switching activity.

FSM based design offers a practical solution to this problem. It represents the complete behaviour of a processor through a defined set of states. Each instruction execution stage is handled at the right time with no redundant state transitions. This reduces switching activity and lowers overall power consumption. When FSM control is combined with clock gating inactive units can be disabled on demand. This leads to significant savings in dynamic power without affecting the correctness of execution.

In this paper, a 16-bit processor with an FSM-based, specifically Mealy, control logic with optimized operation frequency and low power consumption is proposed. Processor design and implementation using Verilog HDL. Power and timing simulation and analysis.

Major objectives of the proposed study:

1. Processor design and development using FSM control.
2. Reduction in dynamic power consumption by clock gating technique using FSM.
3. Achieved an adequate operating frequency.
4. Validate using simulation.

II. LITERATURE REVIEW

Existing research on low power processor architectures highlights a recurring tradeoff between speed and energy efficiency. RISC processors traditionally rely on hardwired control logic to achieve high execution speed. However this approach increases switching activity and contributes to higher power consumption.

FSM based controllers have been shown to simplify hardware complexity while maintaining effective control over processor operations. The Mealy machine variant is particularly suited for processor control because its outputs depend on both the current state and the current input. This allows control signals to be generated faster compared to a Moore machine which relies solely on the current state.

Clock gating is a well established technique for reducing dynamic power consumption. It works by disabling the clock signal to any module that is not active during a given cycle. This prevents unnecessary switching transitions and directly reduces the energy consumed by idle hardware blocks.Prior researches show that FSM-based control logic combined with clock gating can significantly reduce power consumption.

The existing researches only try to find some processors for either high performance and lack of power efficiency or for low power efficiency and limited speed. The present work combined the optimum FSM control logic and clock gating to develop a new low-power processor architecture which also have high speed.

METHODOLOGY

A. Processor Architecture

The design for the proposed processor is based on the following main units: Program Counter (PC), Instruction Memory, Instruction Register (IR), Register File, Arithmetic Logic Unit (ALU), Data Memory, FSM Based Control Unit.

This processor uses a sequential processing approach, controlled by an efficient Mealy FSM. There are 5 states that control this execution:

1. Fetch State
2. Decode State
3. Execute State
4. Memory Access State
5. Write Back State

B. Control unit using FSM

This is the core of the processor and determines the state of the processor in each clock cycle. The output to the other components will be the control signals needed for performing the instructions. During the fetch stage the Program Counter supplies the address to instruction memory and the corresponding instruction is retrieved. In the decode stage the control unit reads the opcode from the fetched instruction and produces the necessary control signals for the operation. The execute stage involves the ALU processing the source operands according to the instruction type. For load and store instructions the processor enters the memory access stage where data is either read from or written to data memory. In the write back stage the final result is stored in the destination register completing the instruction cycle.

C. Power Optimization

Power consumption is reduced through FSM based clock gating. During each execution stage only the functional units that are actively needed receive clock signals. Units that are idle in a given state have their clock gated off. This prevents unnecessary switching transitions in inactive blocks and leads to a measurable reduction in dynamic power consumption.

D. Design Flow

The processor was written in Verilog HDL and synthesized with Xilinx ISE 14.7. Behavioral simulation was performed to verify that instructions executed correctly. Power and timing reports were obtained using FPGA synthesis tool flow.

III. RESULTS AND DISCUSSION

Functional Simulation Results

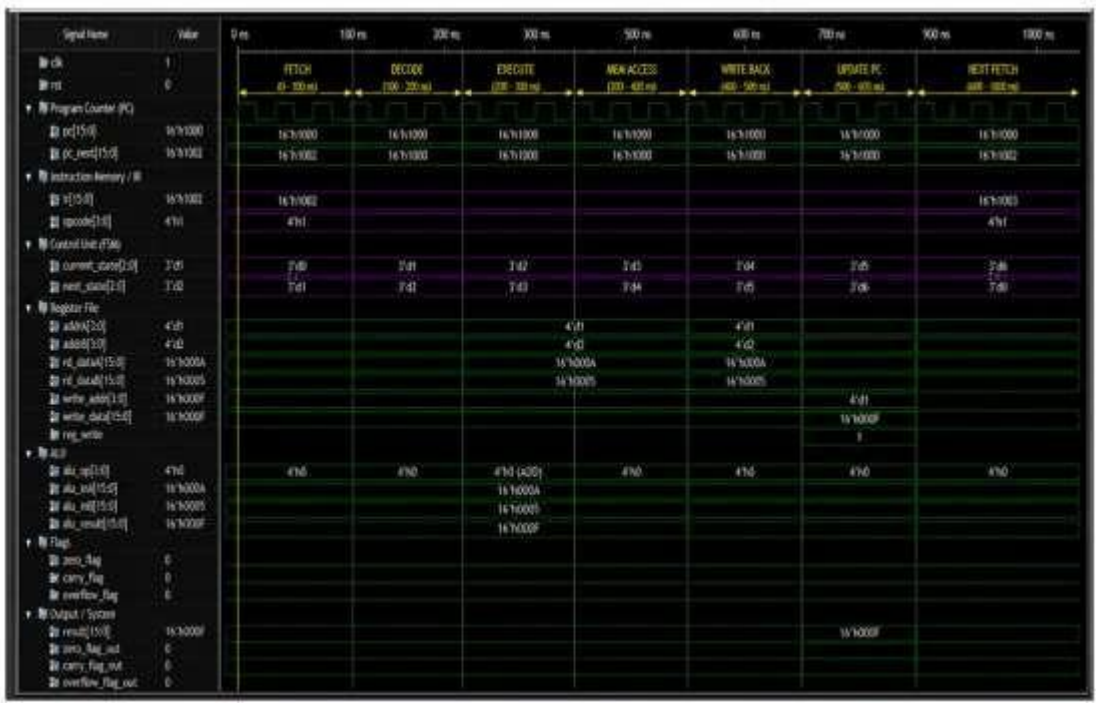

Figure 1:Simulation of output waveforms

The simulation output confirms the proposed processor architecture functions properly. The FSM based 16-bit processor correctly completes instructions at all operation steps as shown in the waveform below. In first step the opcode is fetched to the Instruction Register from instruction memory. In the decode step FSM decodes the opcode and sets the appropriate control signal.

In the execute phase, the ALU processes the operands:

- Operand A = 0x000A
- Operand B = 0x0005

The ALU correctly generates the result:

- Result = 0x000F

Because the instruction is an arithmetic operation there is no data memory access. Write-back stage writes result into the destination register.

After successful completion of the instruction, the Program Counter advances from: PC = 0x1000
PC = 0x1001

This confirms correct sequencing and state transitions within the FSM controller.

Table I: Functional Verification Results

Parameter	**Value**
Operand A	0x000A
Operand B	0x0005
ALU Result	0x000F
Initial PC	0x1000
Final PC	0x1001
Instruction Status	Successful

B. Power Analysis

After synthesis power analysis was carried out.

The overall on-chip power consumed is evaluated as: Total Power = 0.128 W
Dynamic Power = 0.106 W Static Leakage Power = 0.022 W
Below is the breakdown of dynamic power over processor parts.

Table II: Power Consumption Analysis

Component	**Power (W)**
Clock	0.028
Logic	0.024
BRAM	0.020
Registers	0.018
Signals	0.016
Leakage	0.022
Total Power	0.128

Clock power is still minimal, as clock-gating is controlled via FSM. The power savings are mostly owing to the decreased switching activity.

C. Timing Performance

Timing shows good performance. The synthesized processor runs at a maximum clock frequency of: 182 MHz
The design has no timing violations and no negative slack. The post synthesis design goal was: 68 MHz
The operating clock is approx 2.67 times greater than the goal.

Table III: Timing Performance Comparison

Parameter	**Value**
Target Frequency	68 MHz
Achieved Frequency	182 MHz
Timing Slack	0 ns
Status	Timing Met

The large gain in operating frequency demonstrates that the proposed optimized Mealy FSM controller works properly, and has power efficiency and operation speed well balanced.

IV. CONCLUSION

In this article, a high speed and low power 16 bit processor is implemented using FSM-based control scheme. Mealy FSM is used and it is optimized. The FSM control execution of the instructions and the dynamic power dissipation is reduced using clock gating. Processor works correctly as demonstrated by functional simulation which tests all the stages like fetch, decode, execute and write-back.

Power analysis showed the low on chip power consumption (0.128 W) and timing analysis showed high operating frequency (182 MHz) which is higher than the required one (68MHz).

It has shown that FSM based control works well for both speed and power requirements. Pipelined operation, better power management scheme and larger instruction set are potential for future.

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