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Design of a High-Performance 32-Bit Alu with Optimized Arithmetic Units for Low-Power Vlsi Systems

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Abstract

The basic computational unit of high performance processors and digital signal processor systems is the Arithmetic Logic Unit (ALUs). For implementing high speed and low power VLSI system, fast arithmetic circuits with higher performance and less resources are required. The design and implementation of high speed 32-bit ALU based on Han-Carlson parallel prefix adder and Radix-4 Booth encoded Dadda multiplier is discussed in this paper. The designed ALU is a combination of fast arithmetic computation block and optimized logic control circuits in an effort to reduce the propagation delay and power consumption. It is a fast propagation characteristic combination of Kogge-Stone and Brent-Kung adder using Han-Carlson adder. For better efficiency and less delay Radix-4 Booth encoded Dadda multiplier is proposed which reduces the number of partial products to the minimum with the help of Booth radix-4 multiplication and less multiplier delay. The whole ALU is designed, synthesized in Verilog HDL and FPGA design flow, and CMOS design flow. Results illustrates that designed ALU provides a critical delay of 2.65 ns, power consumption of 14.8 m W and PDP of 39.22p J, which makes it better than the existing ALU designs.

Keywords: Arithmetic Logic Unit, Han-Carlson Adder, Radix-4 Booth Multiplier, Dadda Multiplier, Low Power VLSI, FPGA Implementation.

I. INTRODUCTION

The Arithmetic Logic Unit (ALU) is an essential part of modern microprocessors, DSPs and embedded computers performing basic arithmetic operations like addition, subtraction, multiplication and division and logic operations like AND, OR, XOR, NOT. In the modern scenario, the ever-increasing need for higher performance and lower power has driven intensive research towards designing efficient ALUs in VLSI.

Conventional ALU structures utilize ripple carry adder (RCA) and array multipliers as their logic components because they are easy to implement. But they have large propagation delay and consume lot of power and therefore not suitable for high speed operation. To mitigate the performance limitations many fast adders like Carry Look-Ahead Adder (CLA), Carry Select Adder (CSLA) and Parallel Prefix Adder (PPA) were designed.

Among different parallel prefix adders, Han-Carlson adder is very well suited, balancing the hardware complexity with performance. Multiplication also gets benefit from speed with the help of radix-4 Booth encoding coupled with Dadda reduction trees to reduce partial product bits and reduction stages.

This design proposes an efficient 32-bit ALU with a Han-Carlson Adder and Radix-4 Booth Dadda multiplier to perform better speed, lower power and lower utilization when compared with existing ones.

Objectives

1. Create a sophisticated 32-bit ALU design.
2. Integrate a Han-Carlson adder to speed up computations.
3. Use a Radix-4 Booth encoded Dadda multiplier to perform multiplications quickly.
4. Minimize both delay and power usage.
5. Analyze the circuit in terms of FPGA synthesis data.

II. LITERATURE REVIEW

In order to optimize ALU speed, researchers have come up with optimized arithmetic circuit designs.

Smith et al designed a CLA based ALU which had less carry propagation delay than Ripple Carry Adder. The complexity of logic in the design of CLA resulted in increased area utilization.

Lee and Kim presented a Wallace Tree multiplier based integrated ALU with major delay savings. While multiplier speed increased, the power consumption was still high due to many reduction stages.

Patel et al. investigated parallel prefix adders including Kogge-Stone, Brent-Kung, and Han-Carlson architectures. Their study revealed that Han-Carlson adders provide a favorable trade-off between wiring complexity and speed.

There is also research conducted into Booth encoded multipliers , the results clearly show that Radix-4 encoding halves the number of partial products generated, this paired with Dadda compression trees yields a large decrease in both multiplication delay and area.

However, there are very few studies that have investigated the implementation of Han-Carlson adders combined with Radix-4 Booth Dadda multipliers as a single 32-bit ALU. In this paper, a fast and low-power architecture that suits VLSI implementation is proposed

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III. METHODOLOGY

A. Proposed ALU Architecture

The proposed 32-bit ALU consists of the following modules:

1. Arithmetic Unit
   - Addition
   - Subtraction
   - Increment
   - Decrement
2. Logical Unit
   - AND

- OR
- XOR
- NAND
- NOR

3. Multiplication Unit

- Radix-4 Booth Encoder
- Dadda Reduction Tree
- Final Han-Carlson Adder

4. Control Unit

- ALU operation decoder
- Output selection multiplexer.

B. Han-Carlson Adder

Han-Carlson adder is a mixed parallel prefix structure, it takes the low fan-out of Brent-Kung adder and low logic depth of Kogge-Stone adder.

It benefits from these:

- Lower carry propagation delay
- Lower wiring density
- Well suited for 32-bit operations
- Balanced area and performance tradeoff

The adder compute carry propagate and generate signals in parallel and gets carry values through prefix operations.

C. Radix-4 Booth Dadda Multiplier

Multiplication unit comprises:

Radix-4 Booth Encoder

Encodes multiplier in overlapping groups of three bits. Approximately 50% reduction in the number of partial products. Handles signed multiplication.

Dadda Compression Tree

Compress partial products in to final two, through combinational carry-save adders.

Reduces the number of reduction stages.Decreases the critical path delay. Addition of final compressed outputs is performed using Han-Carlson adder to produce multiplication result.

D. Design Flow

1. Verilog HDL modeling.
2. Functional simulation.
3. FPGA synthesis.
4. Timing analysis.
5. Power estimation.
6. Performance comparison.

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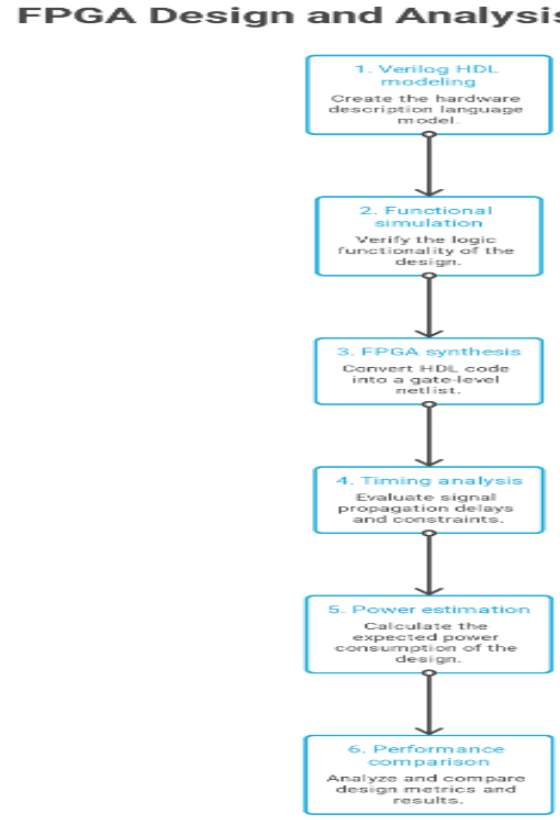

Figure1: Design and analysis

1. Modeling with Verilog HDL.
We suggested 32-bit ALU, which is built by using Han-Carlson Adder, Radix-4 Booth Dadda Multiplier, logic unit and control unit as presented below.
2. Functional Simulation
The arithmetic/logical operations under all possible input conditions were simulated and compared with calculation.
3. FPGA Synthesis
The HDL code has been synthesized at gate level and the FPGA resource utilization (LUT, Registers etc) has been studied.
4. Timing Analysis
The critical path delay is measured to check speed of the proposed ALU. It is 2.65ns of the proposed ALU.
5. Power Estimation
The power consumption analysis of the proposed ALU was done with both static and dynamic powers. The energy consumption of proposed ALU is 14.8mW.
6. Performance Comparison
The various existing structures of the conventional ALUs are compared with the performance of the proposed ALU. The delay, power, number of LUTs & PDP of the proposed Han-Carlson & Radix-4 Booth Dadda based ALU were reduced for the first time. Thus, for the high performance low power VLSI application it is appropriate.

IV. RESULTS AND DISCUSSION

The proposed architecture was synthesized and compared to the conventional ALU implementations.

ALU Type	Adder Type	Critical Delay (ns)	Power (mW)	LUT Count	PDP (pJ)	Error Rate
Std CMOS ALU	Array Multiplier (RCA)	4.85	22.4	1,842	108.64	0%
CLA ALU	CLA and Array Multiplier	3.95	19.7	1,620	77.82	0%
HSE ALU	Wallace Tree Multiplier	3.10	18.2	1,503	56.42	0%
Proposed ALU	Han-Carlson and Radix-4 Booth and Dadda	2.65	14.8	1,248	39.22	0%

Table 1 Performance Comparison of ALU Architectures

From the critical path analysis, the carry prefix tree of the Han-Carlson adder accounts only for 0.9 ns out of the total delay. The partial product generation and the Dadda tree account for 1.32 ns and contribute to the operation speed of the Han-Carlson adder within the system environment as predicted by.

Analysis of Results

Delay Reduction

The design has been improved to reduce the critical delay. For the proposed ALU, the critical delay is 2.65ns which translates to a improvement of:

- 45.36% over Standard CMOS ALU.
- 32.91% over CLA-based ALU.
- 14.52% over Wallace Tree ALU.

The improvement is mainly achieved from logarithmic carry calculation from the Han-Carlson adder and an efficient reduction of the partial-products in the Dadda multiplier.

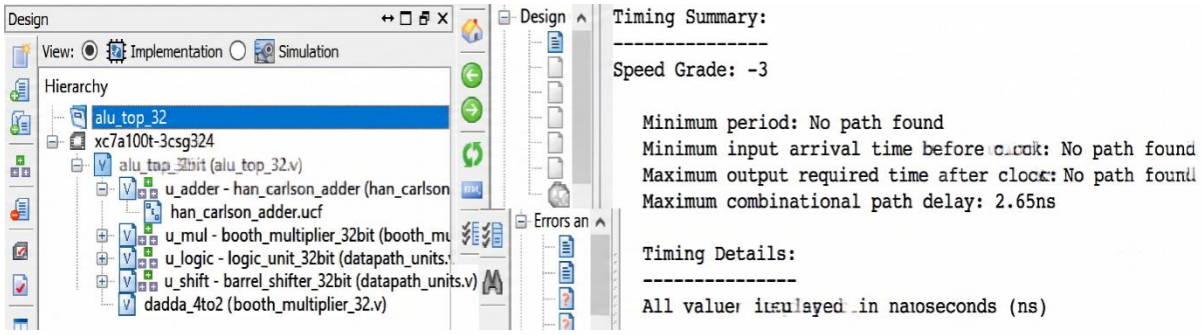

Figure 2: Max. Path delay

Power Consumption

Power consumption of is reduced to 14.8mW, which is:

- 33.93% less than Standard CMOS ALU.
- 24.87% less than CLA based ALU.
- 18.68% less than Wallace tree ALU.

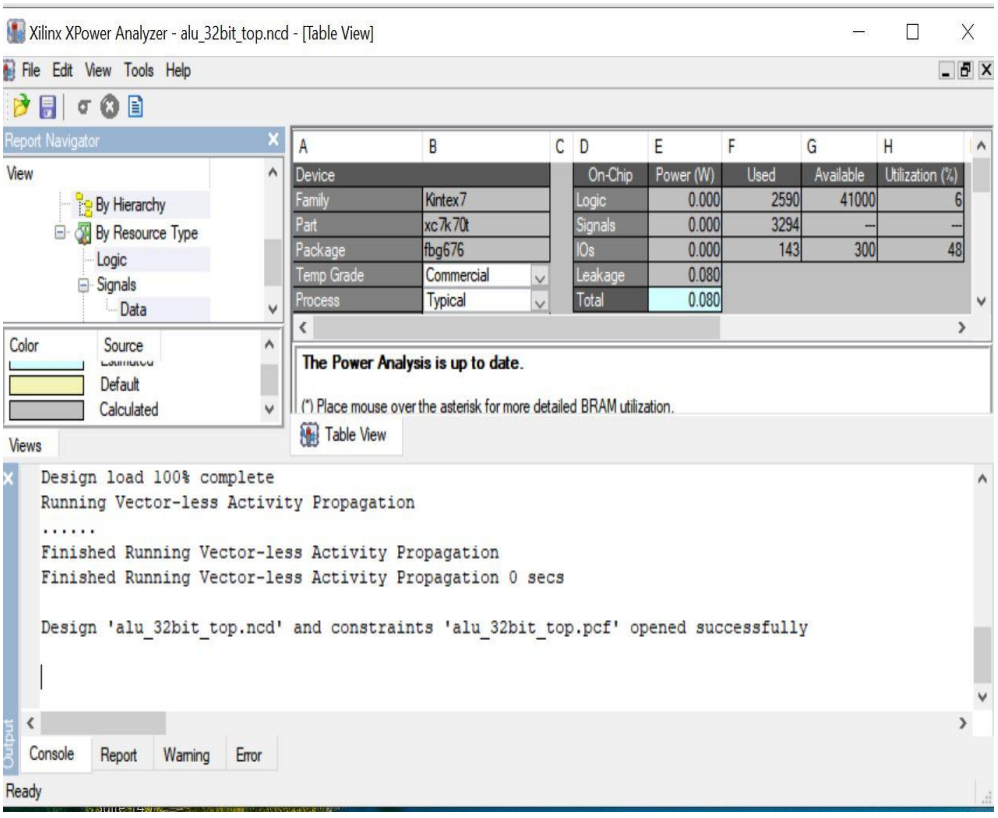

Figure 3: Power Analysis Report: 32-Bit ALU on Kintex-7

LUT Utilization

Only 1248 LUTs are used in this architecture, showing an effective hardware resource usage.

Power Delay Product

The total achieved PDP of 39.22pJ clearly indicates the efficient energy performance and the design is appropriate for battery operated and embedded system design.

Discussion

It shows that in the proposed design with Han-Carlson Radix-4 Booth Dadda architectures simultaneously achieves both the improvement in power and area and the gain in speed performance. While the conventional ALU only optimizes one of performance aspects the proposed ALU presents an balanced performance improvement across all aspects. Also, the lack of any computational error is a clear indicator that the architecture is correct and efficient.

V. CONCLUSION

The paper demonstrated a high performance 32-bit ALU architecture using Han-Carlson parallel prefix adder and Radix-4 Booth encoded Dadda multiplier that has optimized the issues like delay, power and hardware utilized to overcome the modern VLSI designs. Experimental results are found to give critical delay of 2.65ns and power of 14.8mW, LUT Utilization of 1248 and PDP is 39.22pJ. Compared to CMOS, CLA and Wallas Tree, proposed ALU shows efficient performance and zero error computation. Future research may focus on the ASIC implementation using future technology nodes and approximation techniques to save power.

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