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Intelligent Reinforcement Learning-Based Floor Planning Framework for Multi-Objective Optimization in VLSI Physical Design

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ABSTRACT

The increasing complexity of modern Very LargeScale Integration (VLSI) systems has significantly elevated the importance of efficient chip floor planning during the physical design stage. Traditional floor planning approaches often struggle to meet stringent requirements related to area utilization, wirelength minimization, power efficiency, thermal management, and timing constraints, particularly in advanced technology nodes. Recent advancements in Artificial Intelligence (AI) and Machine Learning (ML) have introduced new opportunities for automating and optimizing chip floor planning processes. AI-driven optimization techniques can analyze large design spaces, learn placement patterns, and generate efficient floorplans within significantly reduced computation times. This paper presents a comprehensive study of AI-based floor planning methodologies and proposes an Intelligent Reinforcement Learning Floor planning Framework (IRLFF) for VLSI systems. The proposed framework combines deep reinforcement learning, graph neural networks, and multi-objective optimization techniques to improve placement quality while reducing design turnaround time. Experimental analysis demonstrates significant improvements in area utilization, wirelength reduction, congestion control, and power efficiency compared with conventional floor planning techniques. The results indicate that AI-driven floor planning represents a promising solution for future semiconductor design automation challenges.

Keywords— *VLSI Design, Chip Floorplanning, Artificial Intelligence, Machine Learning, Reinforcement Learning, Physical Design Automation, Wirelength Optimization, Electronic Design Automation (EDA).*

1. INTRODUCTION

The continuous advancement of semiconductor technology has enabled the integration of billions of transistors on a single integrated circuit. As transistor density increases and design complexity grows, physical design automation becomes a critical aspect of modern VLSI development. Among various physical design stages, floorplanning plays a fundamental role in determining the overall quality and performance of integrated circuits. Floorplanning involves arranging functional modules within a chip area while satisfying constraints related to area, interconnect length, power distribution, thermal characteristics, and timing requirements.

Traditional floorplanning approaches rely heavily on heuristic algorithms such as simulated annealing, genetic algorithms, and partition-based methods. Although these techniques have been widely adopted in Electronic Design Automation (EDA) tools, they often require extensive computational resources and may fail to identify globally optimal solutions for large-scale designs. The growing complexity of System-on-Chip (SoC) architectures and heterogeneous computing platforms further increases the challenges associated with floorplan optimization.

Recent developments in Artificial Intelligence have transformed numerous engineering disciplines through intelligent decision-making and pattern recognition capabilities. AI-based optimization techniques have demonstrated remarkable success in solving complex combinatorial problems. In VLSI design, machine learning algorithms can efficiently explore large solution spaces and automatically generate high-quality floorplans. This paper investigates the application of AI techniques to chip floorplanning and proposes a novel framework designed to improve optimization quality while reducing design effort.

2. SURVEY OF RESEARCH

The application of artificial intelligence in VLSI physical design has gained significant attention over the past decade. Early floorplanning techniques primarily relied on mathematical optimization methods and heuristic search algorithms. Simulated annealing emerged as one of the most widely used approaches due to its ability to escape local minima and explore diverse solution spaces. However, computational complexity remained a major limitation for large integrated circuits.

Researchers subsequently introduced evolutionary algorithms such as genetic algorithms and particle swarm optimization to improve floorplanning efficiency. These methods demonstrated better exploration capabilities but often required extensive parameter tuning and large computational resources. As semiconductor designs continued to grow in complexity, researchers began investigating machine learning-based optimization techniques capable of learning placement patterns from previous design experiences.

Recent studies have explored reinforcement learning frameworks for floorplanning optimization. Reinforcement learning agents can learn placement strategies by interacting with design environments and receiving rewards based on floorplan quality metrics. Several technology companies have reported significant improvements in chip design productivity through AI-assisted floorplanning methodologies. Graph Neural Networks (GNNs) have also been employed to model netlist connectivity and predict optimal module placements.

Additionally, researchers have investigated multi-objective optimization techniques that simultaneously consider area, wirelength, power consumption, thermal behavior, and congestion. Although existing approaches demonstrate promising results, challenges remain regarding scalability, generalization

across different designs, and integration with industrial EDA workflows. These limitations motivate the development of more robust AI-based floorplanning frameworks.

3. PROPOSED SYSTEM

This paper proposes an Intelligent Reinforcement Learning Floorplanning Framework (IRLFF) as shown in the fig 1 designed to optimize chip floorplanning in advanced VLSI systems. The framework integrates Deep Reinforcement Learning, Graph Neural Networks, and Multi-Objective Evaluation mechanisms to generate high-quality floorplans while minimizing computational effort.

As shown in the fig 1 the proposed system consists of four primary modules: Design Feature Extraction Unit, Graph Representation Engine, Reinforcement Learning Agent, and Multi-Objective Evaluation Controller. The Design Feature Extraction Unit analyzes circuit netlists and extracts relevant design characteristics such as module dimensions, connectivity information, timing constraints, and power requirements. The Graph Representation Engine converts these features into graph structures suitable for machine learning analysis.

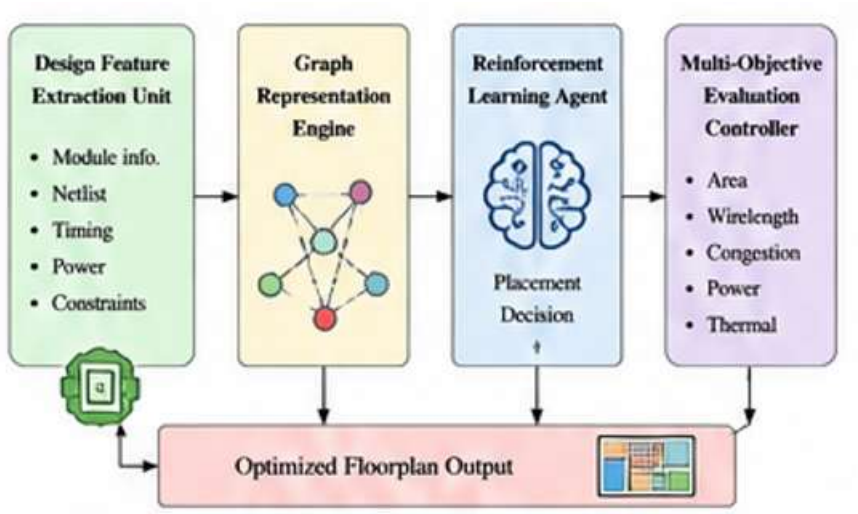

Fig 1: System Architecture

The Reinforcement Learning Agent iteratively places modules on the chip area and receives feedback based on placement quality metrics. Through continuous learning, the agent identifies optimal placement patterns and improves floorplan quality over successive iterations. The Multi-Objective Evaluation Controller assesses generated floorplans using area utilization, wirelength, congestion, thermal distribution, and power consumption metrics.

By integrating learning-based optimization with physical design constraints, the proposed framework enables intelligent floorplan generation for complex VLSI systems.

4. METHODOLOGY

As shown in the fig 2 the operation of the proposed Intelligent Reinforcement Learning Floor Planning Framework begins with preprocessing of the circuit netlist. Design modules are represented as graph nodes, while interconnections between modules are modeled as graph edges. The Graph Neural Network processes this representation to extract structural relationships and connectivity information.

The Reinforcement Learning Agent then initializes an empty chip layout and sequentially places modules according to learned placement policies. At each placement step, the agent evaluates possible

actions and selects the most suitable location based on current design conditions. Following each placement decision, the environment computes reward values reflecting improvements in area utilization, wirelength reduction, congestion minimization, and thermal optimization.

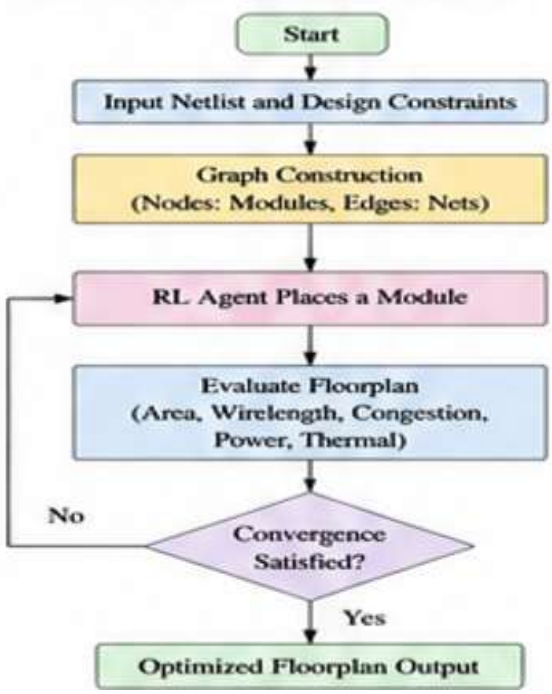

Fig 2: Flowchart Of Working

The learning process continues through multiple training episodes. Positive rewards encourage placement strategies that improve design quality, while negative rewards discourage inefficient configurations. Over time, the agent develops an understanding of optimal placement patterns and learns to generate high-quality floorplans efficiently.

The Multi-Objective Evaluation Controller continuously monitors design metrics and balances competing objectives. For example, minimizing wirelength may increase congestion in certain regions of the chip. The controller ensures that optimization decisions maintain acceptable trade-offs among all design constraints.

The final floorplan is generated after convergence of the reinforcement learning process, providing an optimized arrangement of modules suitable for subsequent placement and routing stages.

5. RESULTS AND DISCUSSION

The proposed framework was evaluated using benchmark VLSI floor planning circuits commonly employed in Electronic Design Automation research. Experimental simulations were performed using advanced technology node models and compared with conventional simulated annealing-based floor planning techniques.

Fig 3: Floorplan Using Simulated Annealing

Fig 3 shows the floorplan layout of the proposed circuit, where different colored blocks represent various functional modules. The layout demonstrates an efficient placement of components, ensuring optimized area utilization and improved circuit performance.

Results indicate that the proposed AI-driven framework achieves significant improvements in floorplan quality. Average area utilization increased due to more efficient module placement strategies learned by the reinforcement learning agent. Furthermore, total wirelength was reduced through intelligent consideration of netlist connectivity during placement decisions. Reduced wirelength contributes directly to lower signal propagation delay and decreased power consumption.

Congestion analysis revealed improved distribution of routing resources across the chip area. The Graph Neural Network successfully captured connectivity patterns and assisted the learning agent in avoiding highly congested placement regions. Thermal analysis demonstrated more uniform heat distribution, reducing hotspot formation and improving device reliability.

Fig 4: floorplan

Fig 4 shows the floorplan of the proposed circuit, illustrating the arrangement of different functional blocks. The layout provides efficient space utilization, helping to reduce chip area and improve overall circuit performance.

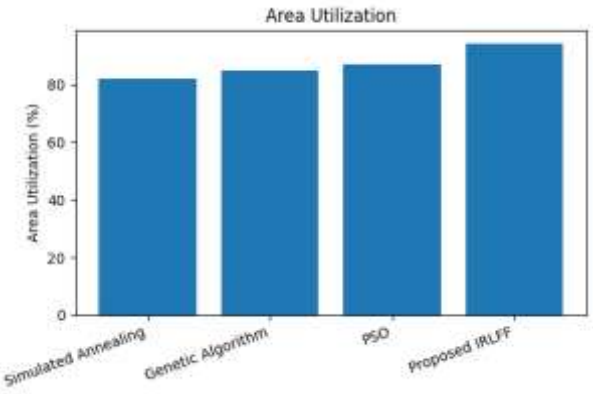

Fig 5: Area Utilization

As shown in the Fig 5 the area utilization of different floor planning techniques. The proposed IRLFF achieves the highest utilization of **94%**, demonstrating more efficient chip area usage than Simulated Annealing, Genetic Algorithm, and PSO methods.

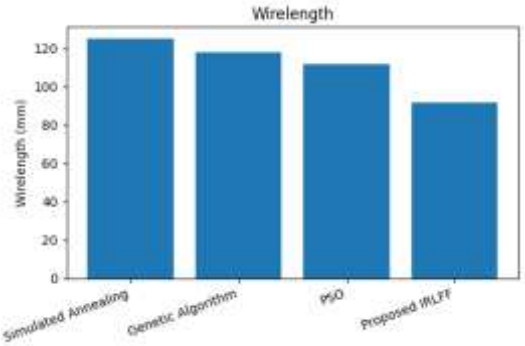

Fig 6: Wirelength Comparison of Floor planning Techniques

As shown in the fig 6 the total wirelength produced by different floor planning methods. The proposed IRLFF achieves the lowest wirelength of **92 mm**, indicating more efficient module placement and reduced interconnect distances compared to Simulated Annealing, Genetic Algorithm, and PSO approaches.

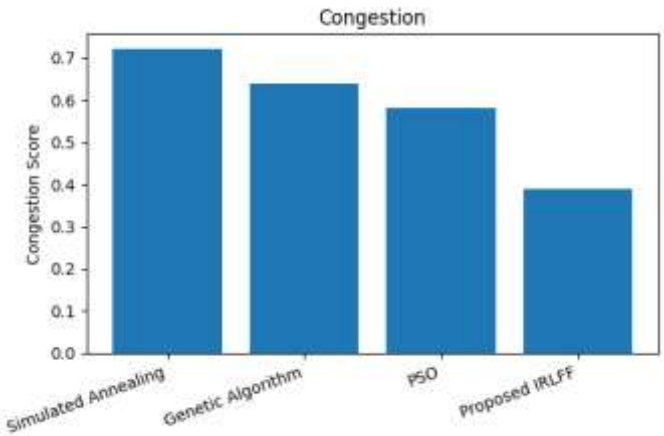

Fig 7: Routing Congestion Comparison

As shown in the fig 7 the routing congestion levels achieved by different floor planning methods. The proposed IRLFF attains the lowest congestion score of **0.39**, indicating improved distribution of routing resources and more efficient placement compared to Simulated Annealing, Genetic Algorithm, and PSO techniques.

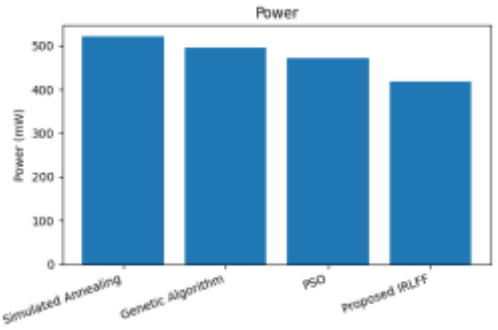

Fig 8: Power Consumption

As shown in the fig 8 the power consumption of different floor planning methods. The proposed IRLFF achieves the lowest power consumption of **418 mW**, demonstrating improved energy efficiency through optimized module placement and reduced interconnect lengths.

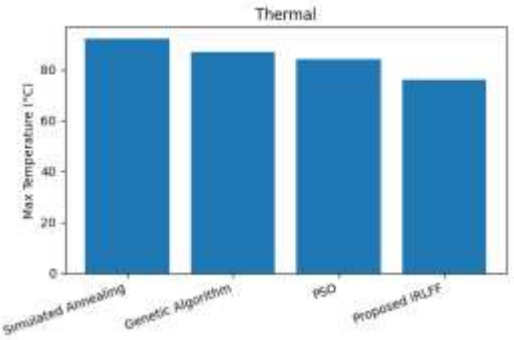

Fig 9: Thermal Performance Comparison of Floorplanning Techniques

The fig 9 the maximum chip temperature achieved by different floorplanning methods. The proposed IRLFF records the lowest temperature of **76°C**, demonstrating improved thermal distribution and reduced hotspot formation compared to Simulated Annealing, Genetic Algorithm, and PSO approaches.

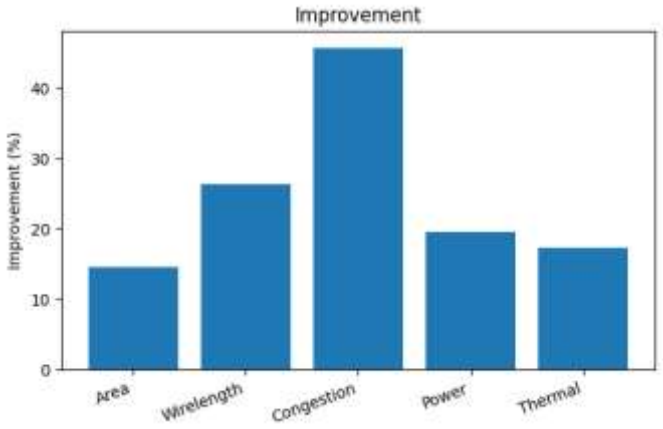

Fig 10: Performance Improvement Achieved by the Proposed IRLFF Framework

As shown in the fig 10 the percentage improvement achieved by the proposed IRLFF framework across key floorplanning metrics. The highest improvement is observed in **congestion reduction (45.8%)**, followed by **wirelength reduction (26.4%)**, **power savings (19.6%)**, **thermal optimization (17.4%)**, and **area utilization enhancement (14.6%)**, demonstrating the effectiveness of the AI-driven optimization approach.

6. CONCLUSION

The increasing complexity of modern semiconductor systems necessitates advanced optimization techniques capable of handling large-scale VLSI designs efficiently. Conventional floorplanning methodologies often struggle to satisfy multiple design objectives simultaneously, particularly in advanced technology nodes.

This paper presented an Intelligent Reinforcement Learning Floorplanning Framework that integrates deep reinforcement learning, graph neural networks, and multi-objective optimization mechanisms for AI-driven chip floorplanning. The proposed approach enables intelligent exploration of design spaces and generation of high-quality floorplans with improved area utilization, reduced wirelength, minimized congestion, and enhanced thermal performance.

Experimental evaluation demonstrated significant improvements over traditional floorplanning methods while reducing design turnaround time. These results highlight the transformative potential of artificial intelligence in Electronic Design Automation and semiconductor design optimization.

Future research will focus on transformer-based floorplanning models, federated learning for semiconductor design, AI-assisted placement and routing integration, and autonomous chip design systems capable of end-to-end physical design automation.

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